ELECTROPLATED COMPLIANT HIGH-DENSITY INTERCONNECTS FOR NEXT-GENERATION MICROELECTRONIC PACKAGING

A Thesis

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ELECTROPLATED COMPLIANT HIGH-DENSITY INTERCONNECTS FOR NEXT-GENERATION MICROELECTRONIC PACKAGING

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“Education is what remains after one has forgotten everything he learned in school” –

Albert Einstein

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LIST OF ABBREVIATIONS

ASF – Amps Per Square Feet

BOE – Buffered Oxide Etch

BOL – Bed of Nails

BGA – Ball Grid Array

C4 – Controlled Collapse Chip Connection

CPW – Co-Planar Waveguides

CSP – Chip Scale Package

CTE – Coefficient of Thermal Expansion

DNP – Distance from Neutral Point

FC – Flip Chip

FCOB – Flip Chip On Board

FEM – Finite Element Methods

FR-4 – NEMA designation Flame Resistant 4

GSI – Giga Scale Integration

GPD – Generalized Plane Deformation

HCF – High Cycle Fatigue

IC – Integrated Circuit

IFC – Interconnect Focus Center

IPC – International Printed Circuit Association

I/O – Input/Output

ITRS – International Technology Roadmap for Semiconductors

LCF – Low Cycle Fatigue

LSI – Large Scale Integration

MSI – Medium Scale Integration

NEMA - National Electrical Manufacturers Association

PDA – Personal Digital Assistant

PEB – Post Exposure Bake

ppm – Parts Per Million

PSD – Particle Size Distribution

PSR – Plastic Strain Range

PTH – Plated-Through-Hole

PWB – Printed Wiring Board

R – Rosin

RA – Rosin-Activated

RMA – Rosin Mildly Activated

RIE – Reactive Ion Etch

RSM – Response Surface Methodology

SCCM - Standard cm^3/min

SEM – Scanning Electron Microscope

SIA – Semiconductor Industry Association

SoL – Sea of Leads

SoPP – Sea of Polymer Pillars

SSI – Small Scale Integration

SMA – Surface Mount Assembly

SMT – Surface Mount Technology

TAB – Tape Automated Bonding

TSI – Tera Scale Integration

TSR – Total Strain Range

ULSI – Ultra Large Scale Integration

UBM – Under Bump Metallization

UV - Ultraviolet

VLSI – Very Large Scale Integration

WLP – Wafer-level Packaging

LIST OF SYMBOLS

A – Experimentally determined constant for Norton creep law or Anand's Model

a – Strain rate sensitivity of hardening/softening for Anand's model; crack length; Solomon's fatigue exponent for 60Sn/40Pb solder

Ag - Silver

C – Factor for Coffin-Manson Model

Factor for Solomon's Model

Factor for Guo's Model

C_1 – Experimentally determined constant for Garofalo creep

Experimentally determined constant for Norton creep

C_2 – Experimentally determined constant for Norton creep

C_3 – Experimentally determined constant for Norton creep

^{o}C – Degree Celsius

Cu - Copper

E – Tensile (Young's) Modulus

G – Shear Modulus

GPa – Giga Pascals

h_o – Hardening/softening constant for Anand's model

k – Boltzmann's constant (1.38×10^{-26} kJ/K)

K – Kelvin

m – Strain Rate Sensitivity of Stress for Anand's model

MPa – Mega Pascals

n – Strain Rate Sensitivity of Saturation used for Anand's Model

Numerical Constant for Solomon's Equation and Guo's Equation

N - Newton

N_f – Cycle Number or Fatigue Life (mean number of cycles to failure)

Ni – Nickel

Pb – Lead

Q – Activation Energy for Creep

R_g – Universal Gas Constant (8.314×10^{-3} kJ/mol-K)

ROT – Rotational Degree of Freedom

s – Internal state variable for Anand's model

s^* – Saturation value of s for Anand's model

$\hat{s}$ – Coefficient for saturation for Anand's model

Sn – Tin

s_o – Initial value of the deformation resistance for Anand's model

T – Temperature in Kelvin

t – Time

T_g – Glass Transition Temperature

Ti – Titanium

U – Displacement

LIST OF GREEK SYMBOLS

Δ - Change in, or Range when used with Strain

α - Coefficient of Thermal Expansion

ε - Axial Strain

ε_e – Elastic Strain

ε_f – Fatigue Ductility Coefficient (Ductility)

ε_p – Inelastic Strain

$\dot{\varepsilon}_c$ – Steady state strain rate

$\dot{\varepsilon}_p$ - Inelastic strain rate

γ - Shear Strain

γ_p - Inelastic Strain

θ – To specify an angle for alignment

ν - Poisson's Ratio

σ - Stress

ξ – A multiplier of stress for Anand's model

SUMMARY

Dramatic advances are taking place in the microelectronic industry. The feature size continues to scale down and it is expected that the minimum feature size on the integrated circuit is expected to reach 9 nm by 2016, and there will be more than 8 billion transistors on a 310 cm^2 chip, according to various available roadmaps. Subsequently, this reduction in feature size would require the first-level input-output interconnects to decrease in pitch size to meet the increased number of transistors on the chip. Also, to minimize the on-chip interconnect delay, development of low-K dielectric/copper will become increasingly common in future devices. However, due to the low fracture strength of low-K dielectric, it is essential that the first-level interconnects exert minimal force on the die pads and therefore, do not crack or delaminate the low-K dielectric material. It is also preferable to have a wafer-level packaging approach to facilitate test-and-burn in and to produce known-good dies. Based on these growing demands from the microelectronics industry, there is a compelling need to develop innovative interconnect technologies.

This thesis aims to develop one such innovative interconnect – G-Helix interconnect. G-Helix is a scalable lithography-based wafer-level electroplated compliant interconnect that has the potential to meet the fine-pitch first-level chip-to-substrate interconnect requirements. The three-mask fabrication of G-Helix is based on lithography, electroplating and molding (LIGA-like) technologies, and this fabrication can be easily integrated into large-area wafer-level fine-pitch batch processing. In this work, the fabrication, assembly, experimental reliability testing and numerical physics-based modeling of the G-Helix interconnects will be presented.

The fabrication of the interconnects will be demonstrated at 100μm pitch on a 20 x 20 mm die in a class 10/1000 cleanroom facility. The wafers with compliant interconnects will be singulated into individual dies and assembled on substrates using Pb/Sn eutectic solder. The assembly will then be subjected to air-to-air thermal cycling between 0°C - 100°C and the reliability of the compliant interconnect will be assessed. In addition to the thermo-mechanical reliability testing, some of the dies with free-standing interconnects will also be used for measuring the compliance of the interconnects by compressing with a nanoindenter. In parallel to the experimental research, a numerical analysis study will also be carried out. The numerical model will use direction-, temperature, time-dependent, and time independent material constitutive properties as appropriate. The thermo-mechanical fatigue life of the compliant interconnect assembly will be determined and compared with the experimental data. Recommendations will be developed for further enhancement of reliability and reduction in pitch size.

CHAPTER 1

INTRODUCTION

1.1. Microelectronics Packaging

Microelectronics, the branch of electronics that deals with miniaturizing components, launched the modern electronic evolution through the invention of the transistor in 1949 by Brattain, Bardeen and Shockley at Bell Labs [Wong 1993]. To be able to achieve high functionality out of the various transistors, integrating the transistors onto a single semiconductor chip was developed by Bob Noyce of Fairchild Semiconductor and Jack Kilby of Texas Instruments in 1959 which subsequently revolutionized the microelectronics industry because it produced the fundamental building blocks for the integrated circuit (IC) [Wong 1993]. This in turn led to the groundwork which provides the basis of all modern electronic products seen today.

In the continual advancement of microelectronics by scaling the transistors, has led to an integration of 1 – 40 transistors in Small Scale Integration (SSI), to over 300,000 transistors in Ultra Scale Integration (ULSI) for modern electronic, and as many as billions or trillions of transistors for Giga Scale Integration (GSI) and Tera Scale Integration (TSI) in the immediate and far futures respectively. Table 1-1 displays the evolution of microelectronics technology.

Table 1-1: Microelectronics Evolution. [Tummala et al., 1997]

Integration Level	Number of Transistors	Typical Function	Typical Number of I/Os
SSI	1 – 40	Single Circuit Function	14
MSI	40 - 400	Functional Network	24
LSI	400 – 4,500	Hand Calculator	48
VLSI ULSI	4,500 – 300,000 Over 300,000	Microprocessor	64 – 300 300+
GSI	1 Billion	Supercomputer	10,000+

As can be seen in Table 1-1 as the number of transistors increases per unit area, the corresponding number of I/Os increases to accommodate it. Therefore, in each package integration level, an increase in the number of transistors leads to an increase in the number of I/Os on the chip. Figure 1-1 displays the progression of the electronic package to meet the needs of increased transistors and I/Os.

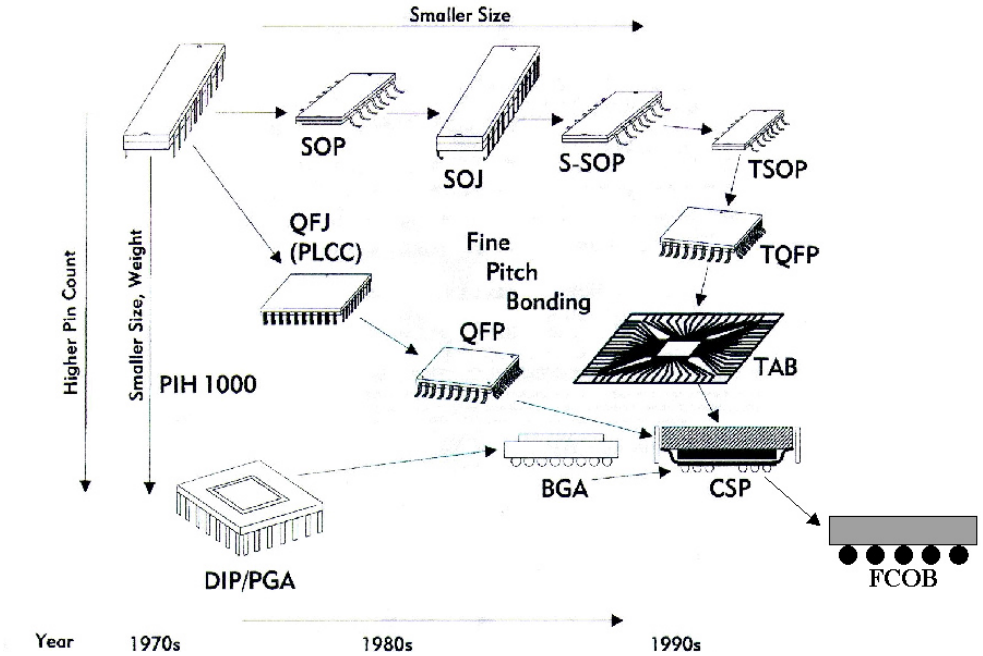


Figure 1-1: Evolution of the microelectronic package. [Tummala et al, 1997]

1.2. Functionality and Hierarchy of Microelectronic Packaging

With the various electronic packages displayed in Figure 1-1, each package has its own unique packaging process, but the main function of all IC packages shown is as follows:

- Power distribution
- Signal distribution
- Heat Dissipation
- Chemical, electromagnetic, and mechanical protection of components and interconnections.

Figure 1-2 visually displays the four main functions of an IC package.

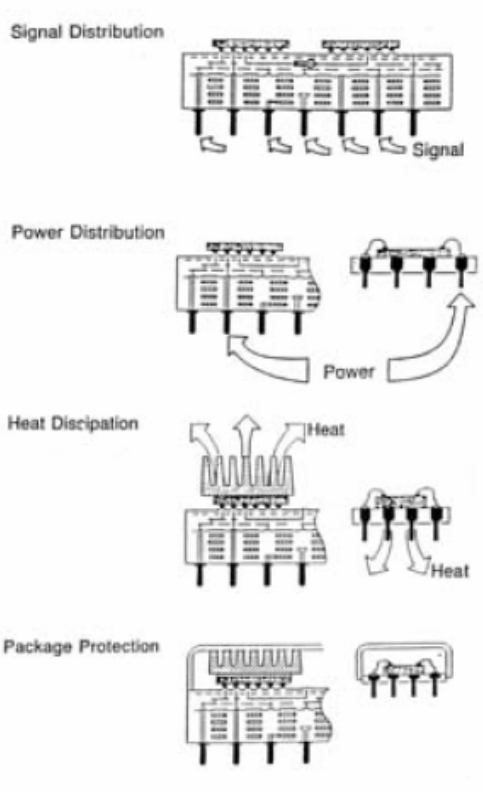


Figure 1-2: Function of a microelectronic package. [Tummala et al, 1997]

Not only does the IC package need to provide the four main functions depicted in Figure 1-2, it also must also perform at a certain level which is determined by the requirements of the electronic product or system.

Microsystems packaging comprises of ICs, passives, and interconnections which can be divided into a six-level microelectronic hierarchy. For the IC to be able to act as a functional entity, the system not only needs transistors, but it also needs resistors, diodes, capacitors, and other components which is subsequently attached by multiple interconnection levels to produce functional systems such as a cell phone or Personal Digital Assistant (PDA). Therefore, Microsystems packaging can be broken down into a six-level hierarchy as displayed in Figure 1-3.

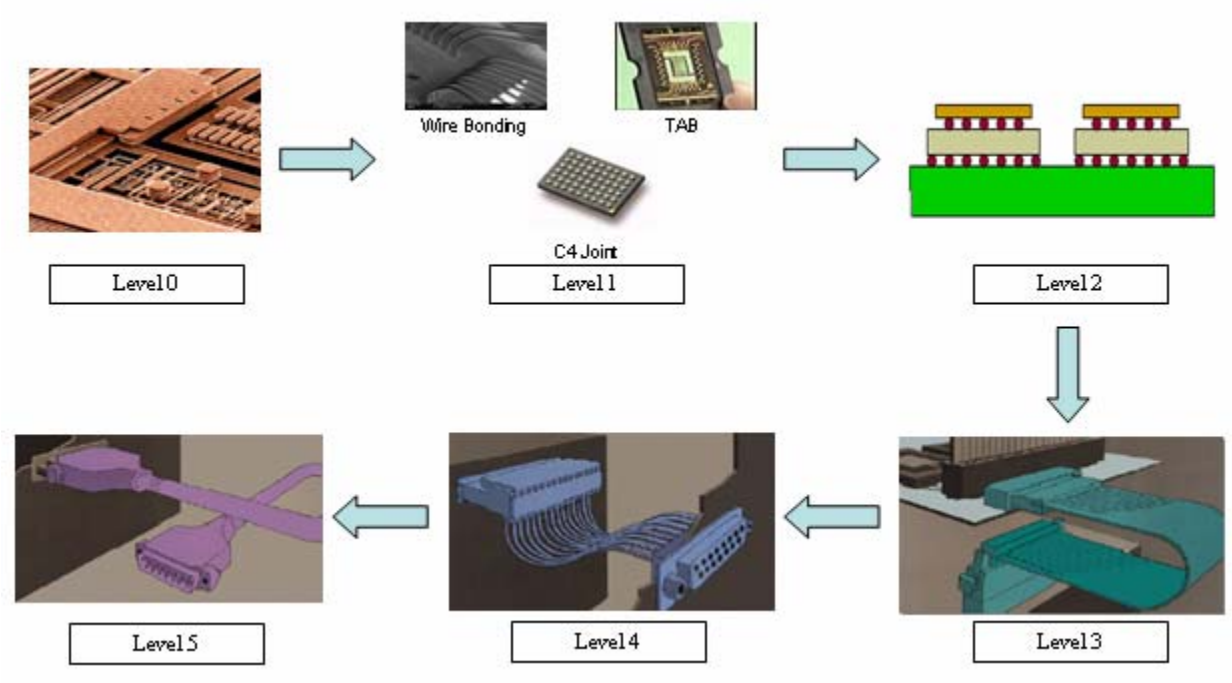


Figure 1-3: Six-Level microelectronic packaging hierarchy [Tyco 2004].

Shown in Figure 1-3, there are six levels in the microelectronic packaging hierarchy. The distinction between each level is as follows:

- Level 0: On-Chip interconnection
- Level 1: Chip-to-Next Level Substrate or Off-Chip interconnect
- Level 2: IC Package-to-PWB
- Level 3: PWB-to-PWB
- Level 4: Subassembly-to-Subassembly
- Level 5: System-to-System

The focus of the work in this thesis will be on the first-level interconnect or also known as the off-chip interconnect.

1.2.1. Level 1 Packaging

Level 1 is described as the chip-to-next level substrate or off-chip interconnect where the function of the interconnect or wiring system is to distribute clock and other signals and to also provide ground/power, to and among, the various circuits/systems functions on a chip. There are many types of IC packages which can be categorized in this level. In general, the IC packages can be classified into two main categories which are: through-hole and surface mount. Figure 1-4 displays examples of the various types of packages classified for through-hole and surface mount technologies.

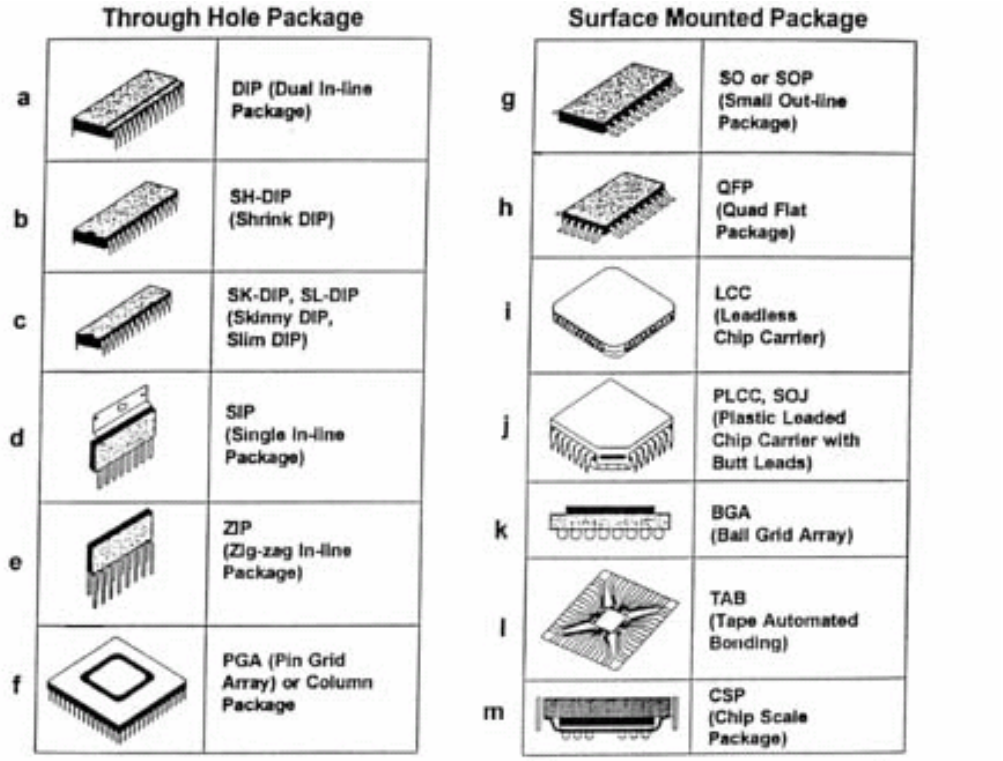


Figure 1-4: Through-hold and surface mount packages. [Tummala, 2001]

With the plethora of IC packages shown in Figure 1-4, the focus of this work will be on a derivative of the Chip Scale Package (CSP) which is known as Flip Chip On Board (FCOB) or Flip Chip (FC). To differentiate between a CSP and FC, CSPs are about 20% larger than the IC and are done as dingle chip packages at the IC level, assembled by standard Surface Mount Technology (SMT), encapsulated and tested [Tummala, 2001]. FC on the other hand is done at the wafer level and bonded with the interconnects face down onto the PWB. In the development of FCOB or FC technology there are some major concerns/challenges that need to be addressed which are as follows:

- High I/O density
- Sound thermo-mechanical reliability
- Good electrical performance

- Good manufacturability
- Low Cost

In conventional packaging, wafer and singulation of the wafer into ICs and the subsequent packaging of the ICs into Ball Grid Arrays (BGA), CSP or other packages are done as two separate parts. To provide FC IC packages at a lower cost, the FC can be taken to another degree by incorporating burn-in and testing at the wafer level. In addition to the BGA, CSP, FC family of packaging, Wafer Level Packaging (WLP) is getting increased attention. WLP is when the IC is packaged at the wafer level, and burn-in and tested at the wafer level. Such a package has the potential of reducing the overall cost of manufacturing microelectronic packages. In this thesis, the investigation will be in a new off-chip interconnect technology which can be used for WLP because we have the potential to perform burn-in and test at the wafer-level.

1.3. The I/O Requirement

To meet the demand for faster, smaller, cheaper, and increased functionality in electronic products such as cell phones, digital cameras, and PDAs, the microelectronic package needs to subsequently improve its performance. Therefore, to improve the system performance, not only does the number of transistors need to increase, but the total I/O count needs to subsequently increase due to the higher demand for the number signals required. This thus leads to a corresponding increase in power and ground I/Os to reduce the electrical noise during the fast circuit switching [Tummala, 2001].

One of the main metrics used to continually push the IC integration path is Moore's law. According to Moore's law the number of transistors on a silicon chip would double every year, which was later revised to every 18-24 months. Based off of

Moore's law, the semiconductor industry has driven the technology envelope from 10 transistors in the 1960s to over 20 million transistors today, and the IC is expected to have over a billion transistors by the end of the decade and be over three centimeters in size [Tummala 2001]. Due to the increased number of circuits (gates) the IC package has, it would require more terminals at their interface. Therefore, the number of I/O interconnects per IC has and will scale at the same rate. Rent's Rule, which is based on observation, with no theoretical foundation) tries to captures and predicts the I/O counts for the future which can be generally expressed as [Tummala et al., 1997]:

$$N = KM^{P} \qquad 1\text{-}1$$

With:

N = number of I/O terminals,

K = average number terminals used for an individual logic circuit,

M = total number of circuits, and

p = Rent's Constant ($0 < p < 1$) which varies depending on the complexity of the IC application.

As stated earlier the main concern and demand for the increase in the number of I/Os is because of the need for more signal terminals for digital applications. Depending on application, different classes of application demand various numbers of terminals for the same number of circuits. Figure 1-5 displays the expected number of terminals versus number of circuits for various applications.

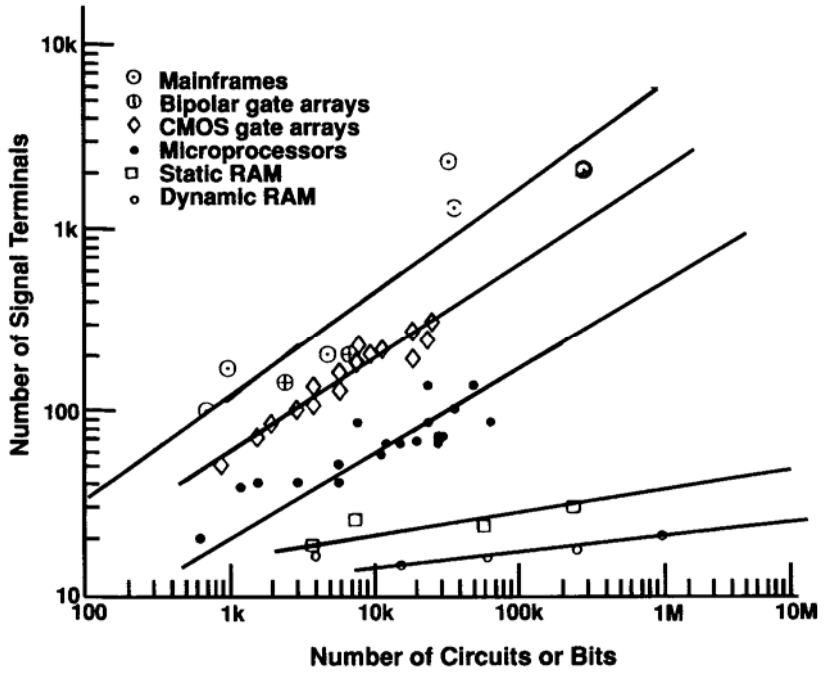


Figure 1-5: Number of Terminals vs. Number of Circuits For Various Applications [Tummala et al, 1997]

It can bee seen from Figure 1-5, supercomputers and mainframes would require the highest expected number of I/Os for a given number of circuits and Dynamic RAM has the lowest requirement of I/Os for a given number of circuits. It should be noted that Rent's rule generally applies for information being conveyed to the assembly of circuits and not necessarily the number of actual lines or terminals. Therefore, if information can be coded on several lines it would result in decreased performance, [Tummala et al, 1997]. Therefore, Rent's rule should be followed to maximize the use of the circuits and prevent performance degradation.

1.4. Off-Chip Interconnect Challenges

As explained in previous sections, the key to improving the performance of the system is not only increasing the number of transistors, but also the number of interconnects between the off-chip interconnect to the package. In addition to I/O count requirements for first level electronic packages, there is also a drive to decrease size of the system package, increase power density, lower cost, and improve silicon efficiency. Where silicon efficiency is defined as the total area of all silicon chips divided by the area of the board. Products such as PDAs, cellular phones, and laptops are example drivers of these trends. Therefore to ensure growth in the semiconductor industry, the Semiconductor Industry Association (SIA) has compiled a roadmap which projects technology requirements for various product categories up to 10-15 years to the future which is called the International Technology Roadmap for Semiconductors (ITRS) [ITRS 2003]. The three most important parameters that the ITRS projects for packaging ICs are the number of I/Os, IC size, and power. Table 1-2 displays the current ITRS roadmap from the year 2003.

Table 1-2: ITRS 2003 Roadmap for Assembly and Packaging [SIA, 2003]

Year of Production	**2004**	**2005**	**2007**	**2009**	**2012**	**2015**	**2018**
MPU/ASIC ½ Pitch (nm)	90	80	65	50	35	25	18
MPU Physical Gate Length (nm)	37	32	25	20	14	10	7
Chip Size (mm^2)							
High-performance	310	310	310	310	310	310	310
Package Pincount [1]							
ASIC (High-performance)	3000	3400	4000	4009	4810	6402	8450
Chip Interconnect Pitch (μm)							
Wire bond – ball	35	30	25	20	20	20	20
Flip chip (area array for cost-performance and high-performance)	150	130	120	100	90	80	70
Peripheral flip chip for hand-held, low-cost, and harsh	60	40	30	20	20	15	15

[1] *Pin counts will be limited for some applications where fine pitch array interconnect is used by PWB technology and system cost. The highest pin count applications will as a result use larger pitches and larger package sizes. The reference to signal pin ratio will also vary greatly dependent on applications with an expected range from 2:1 to 1:4. [ITRS 2003]*

The ITRS roadmap can be used as guidelines by the designer to develop novel technologies that can meet the requirements of future ICs. For instance, it can be seen from the ITRS roadmap that by the year 2018 an area array flip chip for high-performance applications is expected to have a chip interconnect pitch of 70μm with over 8000 I/Os. Therefore, to meet the projections this can be achieved by either utilizing current chip-to-substrate interconnects (wirebonding, Tape Automated Bonding (TAB), solder bump) or developing a novel innovative interconnect technology which can potentially meet the reliability, performance, cost and manufacturability of the next generation package.

1.5. Novel Compliant Interconnect Technology

It can be seen from the ITRS roadmap that in the near and far future, a high density interconnect utilizing conventional or novel interconnect technology is needed to meet the roadmap requirements specified and also be reliable under thermo-mechanical, vibration, and shock loading. For this to occur, developing finer pitch interconnect technologies is necessary to keep pace with developments in IC fabrication and to increase I/O count thus enabling improvements in higher frequency operation and wider buses.

A novel interconnect technology currently being investigated in this thesis approaches the challenge of meeting the criterion of the next-generation package from a compliant approach where during thermal excursions, the interconnect will compensate for the Coefficient of Thermal Expansion (CTE) between the silicon die and PWB. Therefore, the present work concentrates fabrication, assembly, and reliability assessment of fine pitch compliant Off-chip interconnects for packaging applications.

1.6. Outline of Thesis

In the subsequent chapters of this thesis they are organized as follows. Chapter Two presents a literature review on various aspects of off-chip interconnect technology, microfabrication, assembly and thermo-mechanical reliability analysis. Chapter Three covers the objectives and scope of this research. Chapter Four discusses the microfabrication techniques used to construct the compliant interconnect technology. Chapter Five is a discussion of the assembly process and empirical reliability assessment of the compliant interconnect technology. Chapter Six discusses modeling of the interconnect utilizing equivalent beam modeling and how it relates with the mechanical

characteristics of the actual interconnect. Chapter Seven covers thermo-mechanical modeling of the interconnects and correlating those values with the empirical data. Chapter Eight concludes and summarizes this work.

CHAPTER 2

LITERATURE REVIEW

In the previous chapter, the background, present state, general challenges, and motivation to investigate into novel alternative interconnect technology for microelectronic packaging was presented. In this chapter, it will provide a review of various aspects of the first level interconnect technology. Therefore, the chapter is broken up into the following sections:

- Conventional Off-chip interconnect technologies
- Novel Off-chip interconnect technologies
- Microfabrication
- Conventional IC assembly
- Thermo-mechanical Reliability
- Constitutive Relations
- Fatigue Life Prediction Models
- Current Status of G-Helix Compliant Interconnect Technology

2.1. Conventional Off-chip Interconnects

There are three main types of Off-chip interconnect technologies that are readily available out in industry which are: wirebond, Controlled Collapse Chip Connection (C4), or also known as Flip Chip (FC), and Tape Automated Bonding (TAB). Depending on the number and spacing of I/O connections required between the chip and substrate

and the permissible cost, one of the three types of conventional interconnect technologies is preferred.

The most common chip-bonding technology of the three conventional Off-chip interconnect is wirebonding which originated from AT&T's beam lead bonding in the 1950s [Tummala 2001]. The reason of its popularity is because the maximum number of chip connections in products that are designed can be accomplished with this technology. Also, it provides the lowest cost per connection [Tummala 1997]. In this technology, with the use of fine wire, ultrasonic bonding is made between the IC bond pad and the corresponding substrate bond pad. There are two major types of wirebonds used in high volume manufacturing which are: ball bonding and wedge bonding. Ball bonding comprises of 95% of all wirebonding performed in industry using a thermosonic welding technique. The advantages of utilizing wirebonding are because the connection is reliable due to the compliancy derived from the point-to-point process, and is fully repeatable. However, there are limitations to this technology such as the serial processing of each wire; large footprint to provide sufficient room for bonding for high-performance applications, and increased electrical parasitics due to the length to connect from the chip-to-package. Also, it can be seen from the ITRS roadmap that by the year 2009, the minimum pitch requirement for ball bonding plateaus to 20μm. Therefore, the ITRS the technology will be fully matured and no further growth will be seen in this type of technology for high performance applications.

To try and develop a lower cost replacement of wirebonding technology, TAB was first commercialized by General Electric Research Laboratories for use with SSI devices in 1966. This package was based on mounting and connecting ICs onto

metallized flexible polymer tapes [Tummala 2001]. This type of technology received strong attention in Japan where it saw widespread adoption in the 1980s as SMT prospered. Some of the advantages of TAB are that it eliminates large wire loops, ability to handle high I/O count, and ability to burn-in on tape before device commitment. However, some of the disadvantages of TAB are that the package size increases with a increase in I/O count, having no active circuitry under the chip bond pads due to the peripheral interconnection technique, and difficulty in assembly rework [Tummala 2001].

To improve on the latter two Off-chip interconnect technologies in terms of cost, reliability, and productivity, the FC was introduced for ceramic substrate by IBM in 1962. This was converted in 1970 by IBM to the C4 where bare semiconductor chips are turned upside down and bonded directly to the PWB or chip carrier substrate. Interconnection is achieved by two approaches – solder bonding and conductive adhesive bonding. FC technology has been very successful as billions of FC were produced over time where the benefits of the technology were [Tummala 2001]:

- Cheaper than wirebonding as bumping was done as a batch process and at the wafer level
- Improved reliability over wirebonding and beam lead bonding
- Lower electrical parasitics due to shorter connection
- Defective IC can be repairable during assembly or usage

As stated before FC were initially assembled onto ceramic substrates, but as organic carriers proved to be a cheaper, it was subsequently the preferred package to be assembled with. However, this posed an issue because the CTE or an organic carrier

(~17 – 22 ppm/°C) vs. the IC (~3 ppm/°C) would result in poor solder joint reliability. This can be seen from the fundamental fatigue:

$$\gamma_{Outer\ C4\ Solderjo\,\mathrm{int}} = \frac{DNP\left[(\alpha_A - \alpha_B)(T_{\max} - T_{\min})\right]}{H} \qquad 2\text{-}1$$

With:

H = C4 interconnection height

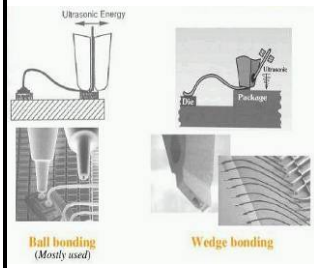
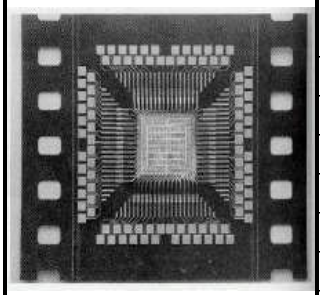
DNP – Distance to neutral point

α_A, α_B = CTE of the two materials where $\alpha_A > \alpha_B$

It can be seen from Equation 2-1 that to decrease the shear strain on the solder joint, it can be done by the following: decreasing the CTE mismatch between the materials, incorporating a smaller die, or by increasing the standoff height of the C4 joint. In reality, with the large CTE mismatch between the die and organic substrate, ever increasing size of die, and continued reduction in interconnect size, it is not feasible to reduce the shear strain induced in the solder joint. Therefore, the interconnects will fail under fatigue under a few accelerated thermal cycles. To address such a solder joint fatigue issue, underfill can be added to couple the chip and substrate over the entire area of the chip thus decreasing the thermo-mechanical stress on the solder and enhance the reliability of the package. The drawbacks to underfill are that once it is dispensed and cured, it eliminates the opportunity of reworkability. Also, in dispensing underfill, when the die size increases and the standoff height decreases, the ability and amount of time to underfill the package may pose an issue. Therefore, increasing the cost to complete the package. Overall, of the three conventional off-chip interconnects, the FC clearly

dominates the other two technologies in terms of electrical parasitics, cost, and reliability. Table 2-1 summarizes the three conventional off-chip technologies.

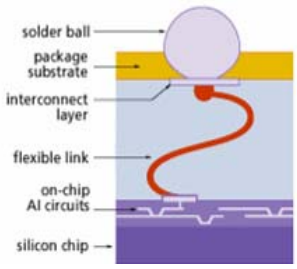
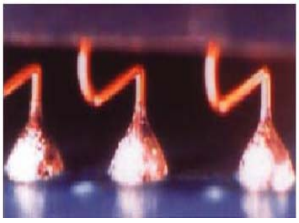
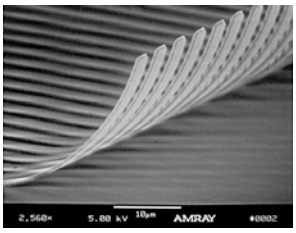
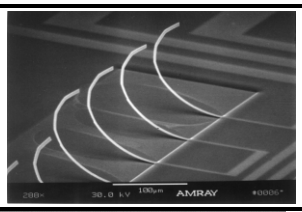
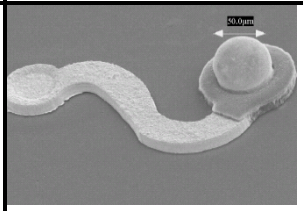
Table 2-1: Summary of Conventional Off-Chip Interconnect Technologies [Zhu 2003].

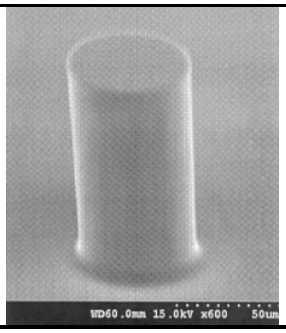
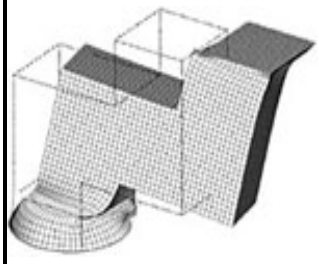
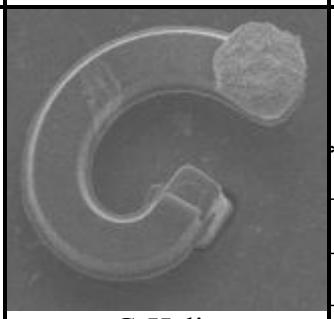
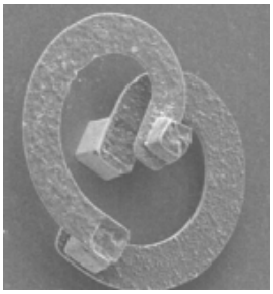
Technology	Illustration	Attributes	References
Wire Bonding		* Au wire (T/C); Al wire (U/S) + Simple, reliable and completely repeatable bond process + Infrastructure is readily available for this technology – Serial processing with slow rate – Large footprint ⇒ large pitch size – Peripheral location ⇒ Low I/O numbers – Long interconnection length ⇒ degrading electrical performance	[Tummala 1997, 2001] [Gilleo 2003] [Qin 2002]
Tape Automated Bonding (TAB)		* Flexible polymer tape with fabricated copper lead and gold plated coating + Gang bonding ⇒ high throughput + Thin, light and fine pitch – Peripheral interconnections – Inflexible and costly process – Complex metallurgy – Additional bumping step – Long parallel interconnections	[Lau 1991] [Tummula 1997] [Gilleo 2003]
Solder Bump/ Flip Chip/ C4 joint		* Stencil printed or electroplated solder material; need UBM as barrier/wetting layer and need solder reflow + Wafer-level batch process + Underfill relieve the stresses/strains due to the CTE mismatch + Fine pitch and high density + Shortest electrical path, highest electrical performance /speed – Additional encapsulating and curing steps for underfill – Not reworkable once underfilled – Stencil printing and reflow at fine pitch is difficult	[Lau and Lee 1999] [Gilleo 2003] [Tummula 2001]

2.2. Compliant Off-Chip Interconnects

In the fabrication of fine pitch interconnects for FC and WLPs they should be developed to meet the needs of electrical as well as mechanical performances. Therefore, there are two paths that could be taken in the design of the interconnect: rigid and compliant. With regards to a rigid interconnect for FC and WLPs, solder bumps have been considered for this realm. Due to finer pitch and decreased stand-off height, the reliability of solder bump interconnect may be incapable of achieving the mechanical requirements alone. Therefore, underfill is needed to reduce the magnitude of the shear strain strains induced in the solder bump. But as the pitch size is continually reduced in the next-generation package, it will be difficult to reflow and attach the solder bumps. Also, the cost and difficulty of dispensing underfill increase. Therefore, investigation into novel interconnect technologies should be done to understand if there are alternative ways to meet the needs of the next generation package. In this section, an innovative approach that is explored is compliant interconnects. Currently, there are seven different types of compliant interconnect technologies which are either commercially available or under study at the research level. The different technologies are summarized in Table 2-2.

Table 2-2: Summary of Current Compliant Off-chip Interconnect Technologies

Technology and Company Name	Illustration	Attributes	References
μBGA® and WAVE® (Sunright)		* S-shaped Cu/Au ribbon bonds + No underfill + Batch fabrication + Reliable – Elastomer encapsulating – Limited planar compliance	[Fjelstad 1998 and 1999] [Kim 2001]
MOST ® (FormFactor)		* Au wire bonds + No underfill + Good compliance – Serial fabrication – Limited pitch and interconnect size	[Novitsky 2000] [Tracy 2000]
Linear Spring and J-Spring (Georgia Tech, PARC and NanoNexus Consortium)	 	* Stress-engineered thin metal + Ultra-fine density + High compliance + Batch fabrication + No underfill – Non-standard sputtering process	[Smith *et al.* 1996 and 1998] [Ma *et al.* 2002]
Sea of Leads (SOL) (IFC, Georgia Tech)	 SOL  SOL w/Air Gaps	* Electroplated Au lead * Low-modulus polymer with air-gap + No underfill + Batch fabrication – High temperature processing – Limited in-plane compliance	[Patel 2001] [Bakir 2001 and 2003] [Dang 2004]

Sea of Polymer Pillars (SoPP) (IFC, Georgia Tech)		* Polymer pillar + Ultra-fine density + Batch fabrication + No underfill	[Bakir 2003 and 2004]
Bed of Nails (BON) (NUS, IME)		* Electroplated Cu lead + No underfill + Batch fabrication – Limited in-plane compliance – Successful fabrication of interconnect has not been shown	[Chrg, 2003]
G-Helix and β-Helix (Georgia Tech)	 G-Helix  β-helix	* Electroplated Cu lead + No underfill + Batch fabrication + > 7mm/N compliance in all directions + Conventional IC fabrication techniques – Comprises of multiple mask processes	[Zhu et al, 2003]

Sunright, which is an independent provider of outsource services for burn-in and test for the semiconductor industry acquired Tessera's manufacturing facility for the μBGA® and Wide Area Vertical Expansion (WAVE™) family of CSPs package in 2001. The operations for the chip scale semiconductor package is currently being produced by Flex2Chip, Inc. To produce the μBGA® compliant interconnects, they are formed by patterning the metal layer on a flexible organic tape. The bond leads on the package are pre-treated so that the die and package expand by several mils. The injection/lifting process produce the compliant three-dimensional spring. Next, a low modulus encapsulant material is injected between the wafer and flexible tape. To connect the CSP to the next level package, solder joints are bumped on the other side of the flexible tape. Therefore, it can be seen that an advantage of this package is that the flexible link embedded in a low modulus compliant layer can absorb the CTE mismatch so it eliminates the need of underfill for the bumped solder [Kim 2001]. Improving on what the μBGA® package, a next generation package called WAVE is produced where die and the package are manufactured and tested at the wafer level. Since there are similarities between this technology and TAB, only a peripheral array can be fabricated. Also, the elastomer layer encapsulating the leads limit the amount of compliance of the interconnects.

Another commercially available compliant interconnect developed by FormFactor Inc. is called the MicroSpring™. The MicroSpring™ interconnect is fabricated using precision micro-machining similar to wirebonding where a specially designed and shaped wirebond is placed at a desired location, and then plating the wire thus transforming the interconnect into a spring. The plating alloy provides the spring strength, while a finish

layer of gold ensures a stable electrical contact [Novitsky 2000]. This technology is scalable and can be optimized for low contact force and reliable connection without the use of underfill. However, a drawback to this technology is that the fabrication of each interconnect is performed in a serial process, and when the number of interconnects is high, it subsequently increases the cost to produce the package.

In a consortium between Georgia Institute of Technology, XEROX Palo Alto Research Center (PARC), and Nanonexus Inc, a compliant interconnect was being developed through sputter depositing and patterning metal with high intrinsic stress gradients and releasing the patterned metal to produce the compliant interconnect [Smith et al. 1996 and Ma et al. 2001]. The range of stress that can be produced in the 80%Mo/20%Cr spring metal is -1GPa to +1GPa. Therefore, a 2 GPa stress gradient can be achieved to allow the interconnect to curl up with the upward bending moment. There are two variations to the spring which are the linear spring and J-Spring where the J-Spring attempts to improve the in-plane compliance that the linear spring lacks. To assemble this interconnect onto the board can be achieved by contact sliding with no solder or underfill. The fabrication of the compliant interconnects incorporates conventional IC fabrication techniques. However, non-standard sputtering techniques will be needed to produce the interconnects.

Interconnect Focus Center (IFC), Georgia Institute of Technology, proposed a compliant interconnect structure called Sea of leads (SoLs) [Patel et al. 2001 and Bakir et al. 2001and 2002]. This interconnect is fabricated at the wafer level to try and extend the economic benefits of semiconductor front-end and back-end wafer-level batch fabrication. The SoL interconnect is comprised of a gold lead and can be fabricated with

or without air gaps. The air-gap is used to improve the vertical compliance for probe contact and other movements due to the CTE mismatch between the chip and printed wiring board. It is also used to reduce the dielectric constant of the interconnect dielectric material [Reed et.al. 2001]. To assemble the interconnects to the next level of packaging, eutectic 63Sn/37Pb solder is used. Overall, the fabrication consists of conventional IC fabrication techniques and has the potential of achieving fine pitch without the use of underfill. However, if the interconnect is constructed with air-gaps, requires processing temperatures at high temperatures (> 400°C). Also, there is limited in-plane compliance.

Another compliant interconnect technology that is currently also being developed at the IFC is the next generation SoL called Sea of Polymer Pillars (SoPP) for electrical, optical, and RF applications [Bakir et.al, 2003 and 2004]. This interconnect is constructed of a low modulus polymer to improve the mechanical compliance, and can be batch fabricated with three masking steps. To serve as an electrical interconnect, a thin layer of metal is deposited on the walls of the pillar, and the thickness of the metal layer is minimal to preserve the compliance of the structure. If the interconnect is utilized for optical interconnects, instead of metalizing the sidewalls, either a surface relief or volume grating coupler is produced on the tip connecting to the substrate to act as a physical traverse optical I/O waveguide. To assemble the interconnect onto the substrate, complementary polymer sockets are fabricated on the substrate to hold the pillars complete the electrical connection or to allow the grating coupler at the tip of the pillar to couple light from the substrate-level waveguide into the pillar so that it may be routed to the chip.

The next type of compliant interconnect technology that is currently being investigated jointly by the National University of Singapore and Institute of Microelectronics called the Bed of Nails (BON). This interconnect is comprised of copper which is bonded directly to the next level with eutectic tin-lead solder. Table 2-2 displays an image of the interconnect. Some of the attributes of BON is that it is fabricated using standard IC fabrication techniques and can be fabricated as a batch process. However, the interconnect does have limited in-plane compliance due to the nature of the geometry and successful fabrication of the interconnect has yet to be shown.

The last type of compliant interconnect is called β-helix and G-Helix where the β-helix is a five mask defined structure and the G-Helix is a three mask defined structure. This compliant interconnect is fabricated based off of conventional IC fabrication techniques (lithography and electroplating). The helix-type off-chip interconnects are designed to have good mechanical compliance in the three orthogonal directions and can accommodate the differential displacement induced by the CTE mismatch between the silicon die and the organic substrate. In the design of the interconnect Response Surface Methodology has been used to optimize the mechanical and electrical performance of the interconnect. Unlike conventional solder, the performance of the interconnect can be manipulated by altering the geometry. Table 2-2 displays some of the attributes of this compliant interconnect technology. In this thesis, a scaled down version, fine-pitch version of the G-Helix will be investigated.

2.3. Microfabrication

Microfabrication entails the creation of devices where at least some of their dimensions are at the micron scale. This type of fabrication begins with utilizing

lithography to “build down” from larger chunks of materials which is also called top-down miniaturization. Photolithography is the most widely used form of lithography where patterns are transferred from masks onto thin films.

To utilize the photolithography process, one of the most well known processes used is LIGA which is a German acronym for Lithographie (Lithography), Galvanoformung (electroplating), and Abformong (molding). This process was first carried out at IBM as early 1975 to make high-aspect-ratio gold structures by plating gold in x-ray-defined patterns. Although the first processes did not carry forth molding in combination with the lithography and plating process, the third piece was realized by Ehrfeld at the Karlsruhe Nuclear Research Center in 1982 thus defining the complete LIGA process. Since the in-house operation of the LIGA process requires X-ray mask fabrication processes and expensive synchrotron processes that are not conveniently available, LIGA-like processes such as Ultraviolet (UV) lithography tools have been developed. In UV photolithography, the wavelengths used to expose the photoresist can range from very short wavelengths of extreme UV (10 – 14nm) to deep ultraviolet (150 – 300nm) to near UV (350 – 500nm). For near UV photolithography, the mercury lamp used to produce the near UV light is broken into two types: g-line (435nm) and i-line (365nm). The photoresist that will be used in this work is constructed for i-line exposures.

Polyimide/metal systems have been applied extensively for applications such as multilevel interconnect technology and multichip packaging [Milosevic 1998, Chakravorty 1984, Rickerl 1987]. Polyimides have also been used as electroplating forms to produce metallic microstructures which was reported in 1993 [Frazier 1993]. In

the selection of a photoresist for LIGA-like processes which can achieve high-aspect-ratio devices (50μm - 500μm), it must have the following attributes: excellent sensitivity, high resolution, low optical absorption, and good thermal and chemical stability. A prominent example is a multifunctional epoxy derivative of bis-phenol-A novolak called SU-8. The negative photoresist was developed and patented by IBM has played a prominent role in miniaturization science [Angelo 1992]. Some of the attributes of SU-8 photoresist are:

- High aspect ratio imaging with near vertical sidewalls
- Near UV (350-400nm) and e-beam imagable
- Resist formulations for film thicknesses from <1μm to >200μms with single spin coat processes
- Superb chemical and thermal resistance

After curing the SU-8 resist, it is highly resistant to solvents, acids and bases and has excellent thermal stability. However, if the application calls for the cured structure to not be a permanent part of the device, removal of the resist can be difficult which requires such equipment as a Reactive Ion Etcher (RIE). Therefore, if the fabrication desires easier removal, another type of resist to complement this photoresist is investigated.

Futurrex which was founded in 1985 produces positive and negative photoresist for microelectronic applications. NR9-8000, a negative acting resist, can be used to produce structures that are at film thicknesses of 0.5 – 120μm using conventional *i*-line UV lithography tools at a 365nm exposure wavelength. One of the advantages that this has over SU-8 is that it soluble in acetone. Therefore, photoresist removal is an easy

task. However, if the structure requires multiple build-up layers that are at temperatures >150°C, the photoresist will break down. Hence, this type of photoresist is ideal low temperature processing.

2.4. Conventional IC Assembly

Surface Mount Technology (SMT) comprises of assembling components such as ICs after the wafer is fabricated and singulated onto the surface of the PWB so that it can be packaged for systems use. Therefore, the three primary functions of an IC assembly are to provide:

- Signal and power distribution of the packaged IC to the system
- Mechanical support to the IC
- Environmental protection

To ultimately assemble the compliant interconnect technology investigated, solder bumps are needed, which can be deposited using several processes on either the interconnect side or the PWB side.

Electroplating is one method to deposit solder on either the end post of the interconnect or on the board side. In preparation for the solder to be electroplated, a polymer photoresist mask is used to control volume and registration. Also, prior to bumping the solder onto either surface, an Under Bump Metallization (UBM) is needed to serve as a compatible layer between the bump metallization (Solder) and final chip metallization (Copper). The function of the UBM is to serve as a adhesion layer, barrier layer, wetting layer and anti-oxidation barrier. Also, the UBM aids in preventing corrosion of the chip metallization due to diffusion of contaminant ionics from the

environment [Tummala 2001]. If solder is to be electroplated onto the end post of the G-Helix, a UBM of nickel is deposited on the surface prior to electroplating the solder.

Another method for deposition of solder is called solder paste screening or printing. To print the solder, a stencil is needed which has a pattern of holes (apertures) for solder paste to be pushed through. A squeegee moves across the stencil to create a downward and forward pressure which subsequently pushes the solder paste through the apertures in the stencil. To obtain better accuracy, paste release and wear resistance, it is critical to have a properly made stencil. In the past, it was sufficient to have a stencil made by chemical etching, but pitch resolutions <250μm was a difficult task to achieve [Tummala 2001]. Therefore, another manufacturing process of the stencil that can be used to achieve fine pitch printing involves nickel electroforming the stencil. By electroforming the stencil, it provides smoother aperture walls, which improves the paste release from the stencil. Also, to achieve fine pitch printing capability requires particle size distribution (PSD) to be <15μm for the solder paste. This is because to be able to fill the stencil aperture, the average aperture diameter/average particle size ratio should be >5 [Manessis 2002], Therefore, this requires a reduction of PSD of 20 – 45μm (Type-3) for conventional solder printing to Type-6 (PSD 5 - 15μm) and Type-7 (PSD 2 - 12μm) solder for pitch requirements of ≤100μm alongside a properly designed electroformed stencil [Jackson 2003].

2.5. Thermo-mechanical Reliability

Reliability is defined as the probability that a component or assembly will be operational for the expected period of use [Tummala 2001]. When microelectronic packages are subjected to actual field use, failures in the product are typically seen at the

system level. However, the cause of the failure are always observed at the component level which is due to thermal, mechanical, electrical, or a combination of these failure modes and mechanisms. To assess the reliability and qualify a product within a reasonable amount of time in a well-controlled environment, accelerated tests can be performed. In these accelerated tests, they are performed to obtain reliability data in a much shorter period of time, and an acceleration factor is used to convert the time-to-failure under accelerated test conditions to the actual time-to-failure under normal usage conditions [Tummala 2001]. A commonly accepted thermal cycling profile for microelectronics is by JEDEC (JESD22-A104-B), test condition J and thermal soak 4, which thermal cycles the package between 0°C and 100°C with fifteen minute dwells [JEDEC 2000]

To supplement the empirical data obtained from performing accelerated tests, virtual reliability modeling can also be used for stress and strain analysis to aid the design engineer to determine the failure modes such as interfacial delamination, solder joint fatigue, die cracking. To assess the reliability of the system, numerical models can be developed to take into account the actual geometry details. To obtain a model that attempts to replicate the performance of the system, material modeling of each component is critical.

2.6. Constitutive Relations

In general, with a change in temperature causes the mechanical properties and performance of materials to subsequently change. Some properties and performance, such as elastic modulus and strength decrease with increasing temperature. Others, such as ductility, increase with increasing temperature. Therefore, in the material modeling of

the various materials in the package, constitutive relations that predict strain as a function of stress, temperature, and time should be taken into consideration.

Since solder is used to assemble the G-Helix to the next-level interconnection, the material has the tendency to creep at room temperature. This is because the absolute temperature is greater than one half the absolute melting temperature. The ratio between the absolute temperature and absolute melting temperature is defined as the homologous temperature in an absolute temperature scale. For instance, 63Sn/37Pb solder at room temperature (20°C) has a homologous temperature of 0.62. Taking this into consideration, the material modeling of solder should include inelastic strains that constitute rate-independent plasticity along with rate-dependent deformation behavior either in an explicit creep equation or combine the inelastic strains into a unified viscoplastic model [Anand, 1985, McDowell 1994].

2.6.1. Time-independent Plasticity

Isotropic hardening and kinematic hardening are two strain hardening rules which are used in plasticity. Figure 2-1 schematically sketches the hysteresis loop for the two types of strain hardening rules.

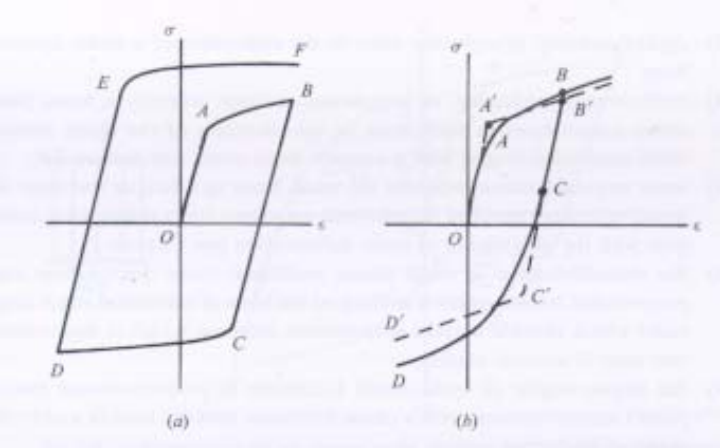


Figure 2-1: Hysteresis Loop Shapes for (a) Isotropic Hardening and (b) Kinematic Hardening [Suresh 2001].

Isotropic hardening is a uniform expansion of the yield surface (after initial yielding) during plastic flow with no shape change or translation. Kinematic hardening represents a translation in the stress space in the direction of the outward normal [Suresh 2001]. To incorporate the Bauschinger effect, kinematic hardening model should be used as it does predict the existence of the effect. Baushinger effect is referred to as after a certain amount of forward plastic deformation in tension or compression, the material will yield at a lower stress when load is reversed than for continued forward deformation [Bauschinger 1886].

The time-independent plastic behavior for the materials can be modeled with either a bi-linear or multi-linear hardening relationship. Multi-linear kinematic hardening is used to represent rate-independent plasticity for copper and solder materials due to the known behavior of the two [Iannuzzelli 1991, Darveaux 1992].

2.6.2. Time-dependent Plasticity

Time-dependent plasticity, otherwise known as creep, is a rate dependent nonlinearity that occurs in materials whose absolute temperature is greater than one half

the absolute melting temperature. Creep can be broken down into three stages which are Primary, Secondary and Tertiary as shown in Figure 2-2.

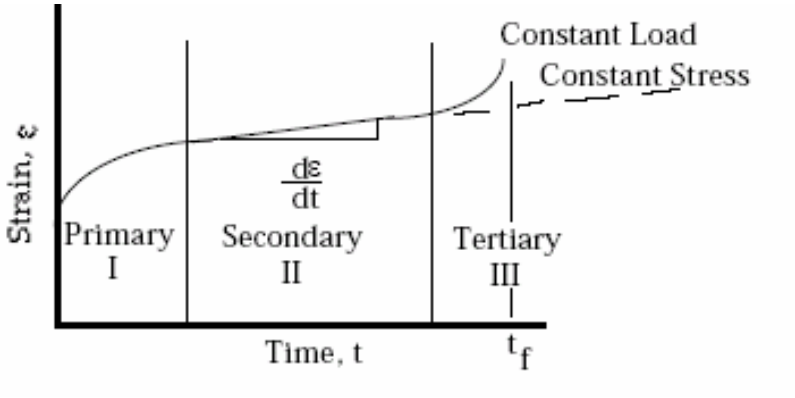


Figure 2-2: Strain time curve for a creep test.

In the primary region, it is characterized by transient creep with decreasing strain rate due to creep resistance of the material to deformation. In the secondary region, the deformation due to creep is at a steady-state and competing mechanism of strain hardening and recovery may be present. In the tertiary region, the creep strain rate begins to increase and necking occurs under constant load.

The steady state creep strain rate for eutectic and near-eutectic solder alloys can be characterized by a Arrhenius-type rate model (also known as Norton creep law) which includes the effect of temperature in the model of Equation 2-2 such that:

$$\dot{\varepsilon}_c = A\sigma^n e^{-(Q/R_g T)} \qquad 2\text{-}2$$

where $\dot{\varepsilon}_c$ is the steady state creep strain rate, σ is the current stress, A and n are experimentally determined material constants, Q is the activation energy for creep, R_g is the universal gas constant, and T is the temperature of the solder in Kelvin.

At higher stresses the power law equation breaks down. Therefore, the strain rate is not dependent on the stress to the power, n [Darveaux 1992]. The power law breakdown region can be subsequently described by the Garafalo relation:

$$\dot{\gamma}_s = C_1 \frac{G}{T}\left[\sinh\left(\alpha \frac{\tau}{G}\right)\right]^n \cdot \exp\left(\frac{-Q}{kT}\right) \qquad 2\text{-}3$$

where $\dot{\gamma}_s$ is the steady state shear strain rate, C_1, n, and α are experimentally determined material dependent constants, Q is the material activation energy for creep, τ is the shear stress, G is the shear modulus, T is the absolute temperature, and k is Boltzmann's constant.

2.6.3. Unified Viscoplasticity Model (Anand's Model)

Viscoplasticity is defined as unifying plasticity and creep via a set of flow and evolutionary equations where a constraint equation is used to reserve volume in the plastic region [ANSYS 1994]. A viscoplastic model which can be incorporated into commercially available software packages is proposed by Anand. This model comprises of a single scalar internal state variable "s", called the deformation resistance, to measure the isotropic resistance offered by the solder to the plastic flow. In this model it assumes no explicit yield condition and no loading/unloading criterion used. Instead, it assumes that plastic flow occurs at all non-zero stress values. Therefore, Anand's model characterizes the inelastic strains with an Arrhenius term for the temperature dependency, and the stress and strain rate dependency of the Garafalo form. The constitutive equation is the flow equation as prescribed in Equation 2-4:

$$\dot{\varepsilon}_p = Ae^{(-Q/RT)}\left[\sinh\left(\xi\frac{\sigma}{s}\right)\right]^{1/m} \qquad 2\text{-}4$$

where $\dot{\varepsilon}_p$ is the inelastic strain rate, A is a pre-exponential factor, Q is the activation energy, R is the universal gas constant, T is the current absolute temperature, ξ is a multiplier of stress , σ is the current tensile stress, m is the strain rate sensitivity, and s is the internal state variable (deformation resistance) and the evolution equation is:

$$\dot{s} = \left\{h_o\left|1-\frac{s}{s^*}\right|^a \cdot sign\left(1-\frac{s}{s^*}\right)\right\}\cdot\dot{\varepsilon}_p; \qquad a>1 \qquad 2\text{-}5$$

where h_o is the hardening/softening constant, a is the strain rate sensitivity of hardening/softening, and s^* is the saturation value of s associated with a given temperature/strain rate pair and is described by Equation 2-6 :

$$s^* = \hat{s}\left[\frac{\dot{\varepsilon}_p}{A}e^{(Q/RT)}\right]^n \qquad 2\text{-}6$$

where $\hat{s}$ is a coefficient for deformation resistance saturation value, and n is the strain rate sensitivity for s saturation.

Anand's model has been shown to provide reasonable results when compared to a combination of plasticity and creep model [Tunga et al, 2002]. To model the material

behavior of solder, nine material constants are needed which are: A, Q, ξ, m, h_o, $\hat{s}$, n, a, plus the initial value of the deformation resistance, s_o.

2.7. Fatigue Life Prediction Models

The following section outlines the fatigue-life prediction models used to evaluate the thermo-mechanical reliability of the compliant interconnect and solder material. Fatigue life models are used to determine the number of cycles that a package can endure before failing. There are two approaches which are: high cycle fatigue (HCF) and low cycle fatigue (LCF). In HCF, it is based off of stress reversals which are in the elastic regime and have not exceeded the yield point. As for LCF, it is based on strain reversals where plastic deformation dominates.

In microelectronic packaging, due to the multi-axial loading that is incurred during thermal excursions, the reliability of compliant interconnect technology is considered to fail under low cycle fatigue where failure is predominately due to plastic strains. To understand the fatigue life of the components in the package, fatigue models have been constructed which fall into the following categories:

- Inelastic strain amplitude (Coffin-Manson-type)
- Strain-energy density-based
- Damage-mechanics-based

In this work, fatigue life based off of inelastic strains will be utilized for characterizing the fatigue life of the compliant interconnect and solder.

2.7.1. Strain Based Predictive Models

The Coffin-Manson model has been widely used to predict low-cycle fatigue life of many metallic materials in terms of the plastic strain range $\Delta\varepsilon_p$ (i.e. the difference between the maximum and minimum plastic strains that occur in the cycle) which is shown below:

$$N_f = \left[\frac{C}{\Delta\varepsilon_p}\right]^{\frac{1}{m}} \qquad 2\text{-}7$$

where $\Delta\varepsilon_p$ is the plastic strain range, N_f is the mean number of cycles to failure, and m and C are numerical constants. This model can be used for 96.5Sn/3.5Ag and 95.5Sn/4Ag/0.5Cu solders. The constants for the two solders are provided in Table 2-3.

Table 2-3: Constants for Coffin-Manson Equation for 96.3Sn/3.5Ag and 95.5Sn/4Ag/0.5Cu Solders [Kanchanomai 2002].

Solder Type	C	m
96.5Sn/3.5Ag	21.9	0.93
95.5Sn/4Ag/0.5Cu	3.7	0.73

Solomon's model which was based on data collected from plastic strain controlled shear test was performed for 60Sn/40Pb solder where the failure criterion was 50% reduction of the load [Solomon 1986]. The equation is based on the plastic shear strain range which is shown in Equation 2-8.

$$N_f = C\Delta\gamma_p^{\,n} \qquad 2\text{-}8$$

where $\Delta\gamma_p$ is the plastic strain range, N_f is the mean number of cycles to failure, and n and C are numerical constants. The constants for 60Sn/40Pb solder is provided in Table 2-4.

Table 2-4: Solomon's Data for Coffin-Manson Equation for 60Sn/40Pb Solder [Solomon 1986].

Coffin-Manson equation:		$\Delta\gamma_p \cdot {N_f}^{\alpha} = \theta$				$N_f = C \cdot \Delta\gamma_p{}^n$	
Temperature, °C	$\overline{T}$	α	$\overline{\alpha}$	θ	$\overline{\theta}$	$C = (\overline{\theta})^{1/\overline{\alpha}}$	$n = -1/\overline{\alpha}$
-50	36.67	0.5	0.51	1.36	1.14	1.29	-1.96
35		0.52		1.32			
125		0.51		0.74			
150	--	0.37	--	0.30	--	not used	not used

Guo has provided another model for 63Sn/37Pb solder [Guo 1997]. The model was derived by machining dog bone specimens from cast ingots which were subsequently annealed and aged to the approximate structure of actual solder joints. Testing was uniaxial total strain controlled which was carried out over 25°C to 80°C. Failure criterion was a 50% load drop of the load. The equation is based off of plastic strain range which is shown in Equation 2-9.

$$N_f = C\Delta\varepsilon_p{}^n \qquad 2\text{-}9$$

where $\Delta\varepsilon_p$ is the plastic strain range, N_f is the mean number of cycles to failure, and n and C are numerical constants. The constants for 63Sn/37Pb solder is provided in Table 2-5.

Table 2-5: Guo's Constants for Coffin-Manson Equation for 63Sn/37Pb Solder [Guo 1992].

Plastic Strain Range	C	n
0.0007 to 0.0025	0.019	-2.04
0.0025 to 0.0255	1.919	-1.35

Engelmaier has developed modifications to the Coffin-Manson equation for reliability prediction of the Institute of Packaging and Circuitry (IPC) copper foil [Engelmaier 1982]. The model is used to predict the fatigue life over the entire elastic-plastic region where the results are based on actual test of foils in reversed bending which was curve-fit. Equation 2-10 displays the model used to predict fatigue life for low to high cycle fatigue [Iannuzzelli 1991].

$$N_f^{-0.6} \times \varepsilon_f^{0.75} + \frac{0.9}{E}\sigma\left[\frac{e^{\varepsilon f}}{0.36}\right]^{0.1785\log_{10}\left[\frac{10^5}{N_f}\right]} = \Delta\varepsilon = TSR \qquad 2\text{-}10$$

where N_f is the mean number of cycles-to-failure, ε_f is the fatigue ductility coefficient (ductility), σ is the ultimate tensile strength, E is the Young's modulus, and $\Delta\varepsilon$ is the total strain range.

When the cycles to failure is low, such as for LCF, the plastic component in Equation 2-10 has a dominant effect. Therefore, the elastic component is removed from the model and can be rewritten as [Iannuzzelli, 1991]:

$$N_f^{-0.6} \times \varepsilon_f^{0.75} = \Delta\varepsilon_p \qquad 2\text{-}11$$

where N_f is the mean cycles to failure, $\Delta\varepsilon_p$ is the plastic strain range, ε_f is the fatigue ductility coefficient (ductility). The fatigue ductility coefficient ranges from 0.15 – 0.3 [Prabhu 1995]. This model has been used and verified by Iannuzzelli for 12 - 50μm thick Plated Through Hole (PTH) on laminate materials.

2.8. Current Status of G-Helix Compliant Interconnect Technology

Helix-type compliant off-chip interconnect is a new interconnect concept which could be a potential solution to the long term size, fabrication, performance, reliability, and cost requirements for the next-generation package. In the previous work, the research focused on design and optimization and theoretical reliability assessment, and limited fabrication of 200μm pitch beta-helix and G-Helix free-standing interconnects was investigated [Zhu et al., 2003].

G-Helix is a layer-by-layer electroplated structure. Shown in Figure 2-3 is the schematic of a G-Helix interconnect and the actual interconnect fabricated.

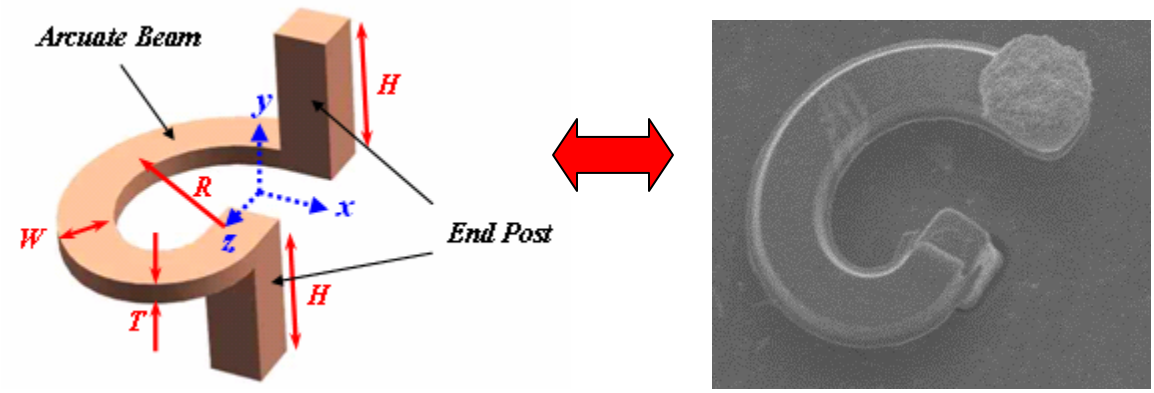


Figure 2-3: Schematic of a G-Helix Interconnect.

The G-Helix interconnect consists of an arcuate beam and two end posts. The arcuate beam is incorporated into the design to accommodate the differential

displacement in the planar directions (*x* and *z*). The arcuate beam is designed with smooth curvature to avoid sharp corners eliminating stress concentrations, and thus to improve the long-term reliability of the structure [Zhu 2003]. The two end posts connect the arcuate beam to the die and to the substrate. The total height of the two posts determines most of the standoff height between the die and the substrate.

In our previous publications [Zhu, Ma, Lo, and Sitaraman 2003], we have used response surface methodology to understand how the four geometric parameters contribute to the performance of the interconnect. The four geometric parameters are: the mean radius of the major part of the arcuate beam (*R*), the height of the two posts (*H*), and the width (*W*) and the thickness (*T*) of the arcuate beam. The response of the interconnect based on the variation of the various geometric parameters is summarized as follows:

Mechanical Characteristic:

↑ R ➲ ↑ Compliance *x, y, z*

↑ H ➲ ↑ Compliance *x, z*

↔ Compliance in *y* stays relatively the same

↑ T ➲ ↓ Compliance *x, y, z*

↑ W ➲ ↓ Compliance *x, y, z*

Electrical Characteristic:

↑ R ➲ ↑ Self-inductance, Resistance

↑ H ➲ ↑ Self-inductance, Resistance

↑ T ➲ ↓ Self-inductance, Resistance

↑ W ➲ ↓ Self-inductance, Resistance

As seen, when a geometric parameter was changed to enhance the mechanical compliance, the electrical parasitic also increases. In other words, a desirable change in mechanical compliance will result in an undesirable change in electrical performance, and vice versa. Therefore, a Response Surface Methodology (RSM) is used to optimize the design of the G-Helix such that the mechanical compliance, electrical parasitics, and thermo-mechanical stresses are kept within acceptable limits. From previous work, the limits for the compliant interconnect are shown below:

$$C_d \geq 10.4\ {}^{mm}\!/_{N}$$

$$C_y \geq 7.1\ {}^{mm}\!/_{N}$$

$$\sigma_d^{von,\max} \leq 173\ MPa$$

$$\sigma_y^{von,\max} \leq 173\ MPa$$

$$0.017\ nH \leq L_{self} < 0.07\ nH$$

$$0.7\ m\Omega \leq R < 50\ m\Omega$$

Where C_d is the diagonal mechanical compliance, C_y is the vertical mechanical compliance, $\sigma_d^{von,\max}$ and $\sigma_y^{von,\max}$ is the maximum von Mises stress when a load is applied

in the diagonal and out of plane direction respectively, L_{self} is the self inductance of the G-Helix, and R is the electrical resistance of the interconnect [Zhu et al., 2003].

Treating all of the above responses with the same importance or with the same weight, an optimized geometry is obtained using Design-Expert®. The numerical optimization algorithm is based on Nelder-Mead method [Zhu et al., 2003]. Using design optimization, a set of resulting optimized G-Helix structure was produced, and Table 2-6 displays the optimized design variables for the compliant G-Helix interconnect.

Table 2-6: Optimized design variables for compliant helix interconnect.

	R (μm)	H (μm)	W (μm)	T (μm)
G-Helix	38	35	11	8

Table 2-7 lists the corresponding responses values from the optimized G-Helix interconnect. When the Finite Element Method (FEM) simulation results are compared to the values obtained through the regression models (RSM), the errors are within 15%.

Table 2-7: Mechanical and Electrical Characteristics of the Optimized G-Helix Interconnect.

	RSM	FEM	Error (%)
C_d	10.198	9.068	12.46
C_y	11.148	10.149	9.84
$\sigma_d^{von,\max}$	169.84	175.55	3.25
$\sigma_y^{von,\max}$	161.49	172.06	6.14
R_{GH}	49.81	43.63	14.16
L_{GH}	0.07704	0.08989	14.30

CHAPTER 3

OBJECTIVES AND APPROACH

Advances in compliant off-chip interconnects have achieved great strides. G-Helix, an electroplated compliant chip-to-substrate interconnect has the potential for accomplishing low-cost, easy-to-fabricate, wafer-level packaging. In the continual drive in the industry for miniaturization of the package, it is essential that the Off-chip interconnect scale down and meet the finer pitch requirements, electrical and thermo-mechanical performance.

3.1. Gaps in Previous Work

Based on the literature review and previous work on lithography-based compliant off-chip interconnects, some important gaps that which need to be addressed for the G-Helix compliant off-chip interconnect are as follows:

- Orientation effects on the stress state of the interconnect during assembly.
- Scaling of interconnects down to a finer pitch.
- Empirical characterization of mechanical response (force vs. displacement) of G-Helix to characterize the mechanical compliance and yield of a single interconnect.
- Successful assembly of free-standing interconnects have yet to be achieved.
- Experimental assessment of thermo-mechanical reliability.

3.2. Objectives

The primary objectives of this research are to fabricate, assemble, and assess the reliability of 100μm pitch compliant G-Helix interconnects. The fabrication of the compliant interconnect will be accomplished in a class 10/1000 cleanroom. The results from the numerical models, which characterize the actual layout of the assembly, will be used to assess and understand the mechanics of the compliant interconnect's deformations and estimate the fatigue life. The numerical results will also be subsequently validated with the experimental data obtained.

The specific objectives of this work are as follows:

- To scale down the fabrication of the interconnects to a pitch of 100μm utilizing LIGA-like techniques.
- Modify and enhance the fabrication techniques to improve yield.
- Experimentally determine the mechanical compliance of the free-standing interconnect and compare with theoretical results.
- Experimentally assess the overall integrity and reliability by subjecting the interconnect to various deformations.
- Assess various methodologies to assemble the compliant free-standing interconnects and successfully assemble the compliant interconnects on substrates.
- Empirically investigate the thermo-mechanical reliability of the assembly.
- In parallel to experiments, quarter-symmetry and GPD assembly models are developed to predict the thermo-mechanical reliability of the interconnects.

- Use the models to assess leaded and lead-free solder attachment reliability.
- Assess the effects of orientation on the stress state of the compliant interconnect on the die during assembly.

3.3. Approach

To achieve the objectives, the following approach has been employed:

- LIGA-like microfabrication to fabricate freestanding high aspect-ratio metallic microstructures. It includes photolithography, molding, electroplating and releasing. The fabrication of peripheral-array wafer-level helix-type compliant interconnects has been carried out based on LIGA-like processes.
- Characterize compliance with a nanoindenter
- Assess various techniques to assemble the G-Helix onto the substrate.
- Assess leaded and lead-free solders to characterize the thermo-mechanical performance of the two types.
- Using strain based damage metrics to understand the fatigue life of the package where time and temperature dependent non-linear, and direction dependent material properties are incorporated into the numerical model.
- Conduct air-to-air accelerated thermal cycling to determine the fatigue life of the compliant interconnect and to also validate the damage-metric based fatigue life models extrapolated from the numerical models.
- Quarter symmetry models with equivalent beam

CHAPTER 4

MICROFABRICATION

Microfabrication entails the creation of devices where at least some of their dimensions are at the micron scale. This type of fabrication begins with utilizing lithography to "build down" from larger chunks of materials which is also called top-down miniaturization. Photolithography is the most widely used form of lithography where patterns are transferred from masks onto thin films. To fabricate high aspect ratio structures (ratio of height:width of structure), LIGA-like processes can be utilized. In this chapter, the design of the wafer, and scaling the fabrication of the G-helix compliant interconnects down to 100μm pitch utilizing LIGA-like processes will be discussed. Micrographs of the fabricated peripheral arrayed free-standing structures will be presented. Also, characterization of the interconnects will be presented.

4.1. Silicon Wafer

The G-Helix is fabricated onto a 6" wafer where each die pad footprint matches the organic substrate to which each singulated die will subsequently be assembled onto. The wafer has a total of sixteen 20 x 20mm dies and each die consists of a three-row peripheral array at a pitch of 100μm. Figure 4-1 displays the wafers used to fabricate the compliant interconnect structures.

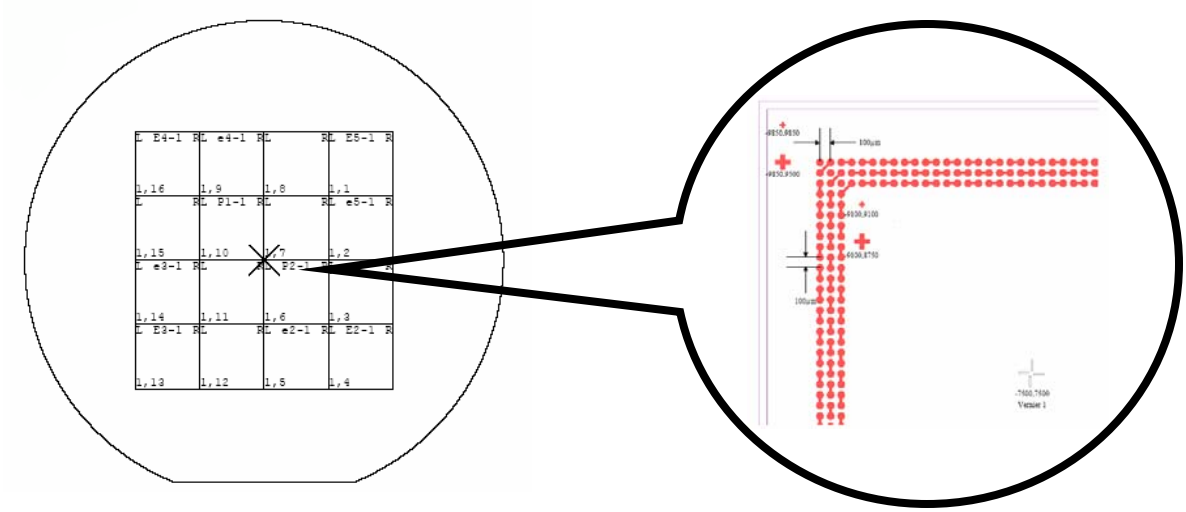


Figure 4-1: Schematic of the Wafer Used to Fabricate the G-Helix.

With regards to each individual die on the wafer, they have been designed to assess thermo-mechanical reliability of the G-Helix interconnects. To monitor the thermo-mechanical performance, daisy chains have been incorporated for each row of the die. A layer of BCB covers the daisy chain and only the copper pads are exposed for subsequent fabrication of the G-Helix. Figure 4-2 displays the cross-section of the wafer.

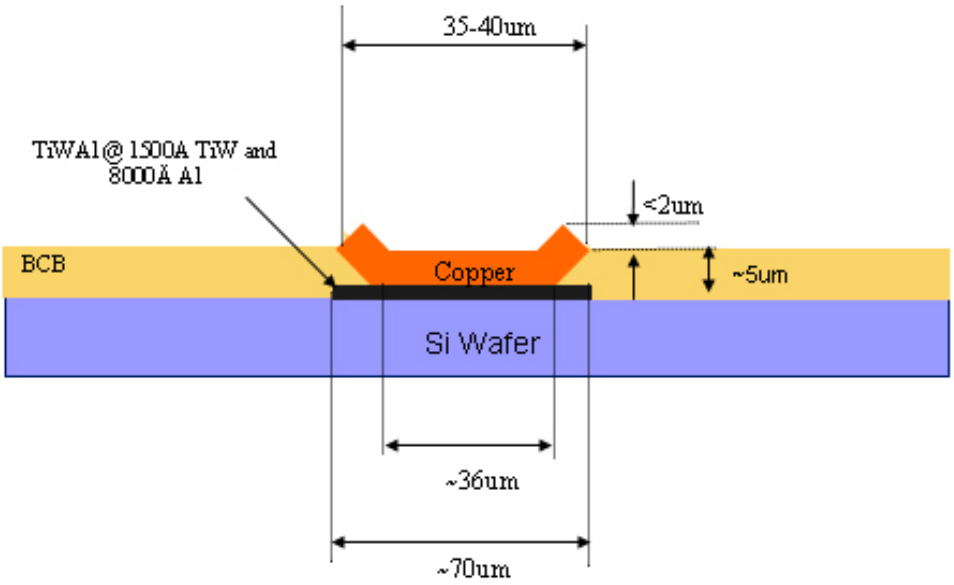


Figure 4-2: Cross-sectional View of Si Wafer used to Fabricate the G-Helix Interconnect.

4.2. Design of Masks

To fabricate the various features of the G-Helix onto the silicon wafer, glass masks which are transparent to UV light is used. The glass mask comprises of an absorber pattern metal (~800 $\mathring{A}$ thick chromium layer) which define the features of the G-Helix. The mask is placed in direct contact with the photoresist-coated surface which is subsequently exposed to UV light. The chromium pattern on the photomask is opaque to UV light, whereas the glass is transparent to UV light which subsequently exposes photoresist.

The definition and fabrication of the G-Helix comprises of a 3-mask process. Therefore, there are three different mask layers to produce three different patterns where the first layer defines the base post, the second defines the arcuate beam, and the third layer defines the top post. AutoCAD® is used to construct the geometry for each mask step of the G-Helix. Figure 4-3 displays the mask layout of the 100μm pitch design.

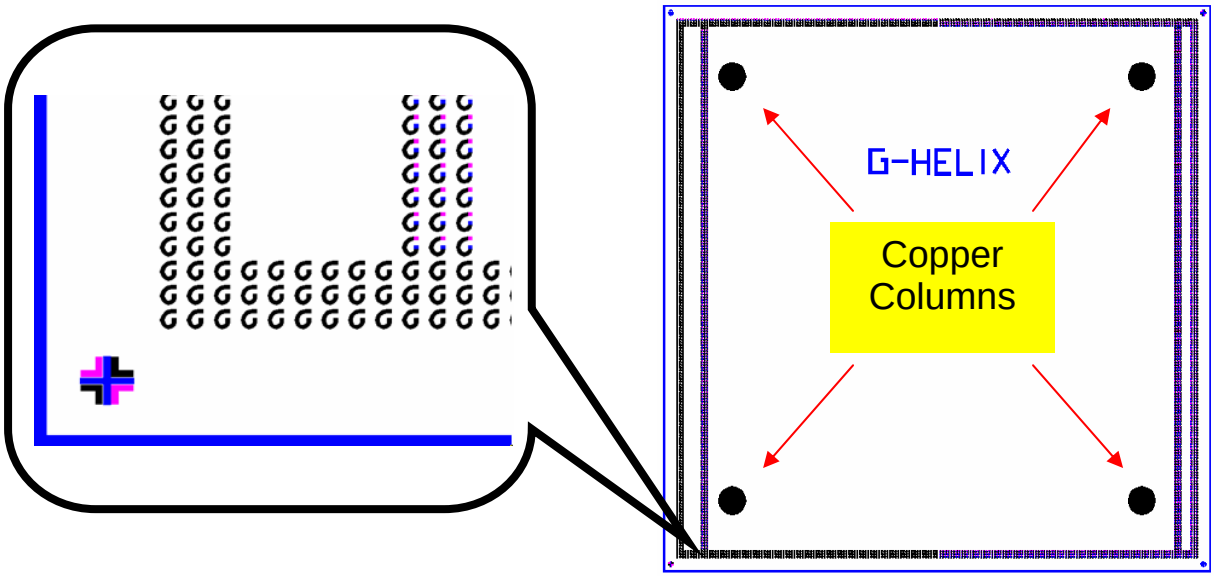


Figure 4-3: Mask Layout of G-Helix on a 20 x 20mm Die.

Alignment marks are designed on the corners of each die to aid in the alignment of the next mask process and to align the die with the next level substrate during assembly. When assembly force is used, it is necessary to ensure that the compliant interconnects do not plastically deform. Therefore, copper columns of larger diameter, as shown in Figure 4-3, were included in the fabrication process. The definition of the copper posts is only defined on the first and second masks. These copper columns would serve as "stoppers" when force is applied during assembly and/or heat-sink attachment. The diameter of the "stoppers" is one millimeter in diameter.

4.3. Photoresist

To fabricate the high aspect ratio structures utilizing LIGA-like processes, selection of either negative or positive photoresist is first made. If negative photoresist is used, then the exposed area on the wafer is cross-linked by UV radiation and the unexposed area can be removed by immersing the photoresist into a developer. If the photoresist is positive, then the exposed area is weakened by UV radiation and it can be etched away by exposing the photoresist to a specific solvent. The mask has to be designed according to the positive or negative response of the photoresist to the UV radiation. In this work, the mask was designed to be used with a two types of negative photoresist: SU-8 and NR9-8000. Both types of resist utilize i-line lithography which means that photolithography uses 365 nm wavelength UV radiation for exposure.

SU-8, a multifunctional epoxy derivative of bis-phenol-A novolak was developed and patented by IBM, has played a prominent role in miniaturization science [Angelo 1992]. This negative photoresist has high optical transparency and is designed for micromachining where a thick chemically and thermally stable image is desired.

Therefore, during electroplating the structures, SU-8 is resistant to acidic and alkaline solutions as well as some solvent-based solutions. SU-8 also has high optical transparency above 360nm thus producing high aspect ratio, near vertical sidewalls. Another attribute of SU-8 is the inherent ability to self-planarize during soft-baking to eliminate an edge bead and provide good contact between the glass mask and photoresist during photolithography. After curing the SU-8 resist, it is highly resistant to solvents, acids and bases and has excellent thermal stability. However, if the application calls for the cured structure to not be a permanent part of the device, removal of the resist consists of dry etching in a RIE.

Futurrex NR9-8000 is a negative, polyhydroxy-styrene based photoresist designed for i-line applications. The negative acting resist can be used to produce structures that are at film thicknesses of 0.5 – 120μm using conventional *i*-line UV lithography tools at a 365nm exposure wavelength. One of the advantages that this has over SU-8 is that it soluble in acetone. Therefore, photoresist removal is an easy task. However, if the structure requires multiple build-up layers that are at temperatures >150°C (i.e. DC Sputter), the photoresist will break down. Hence, this type of photoresist is ideal low temperature processing.

4.4. Fabrication of the G-Helix Interconnect

The fabrication process of the wafer-level interconnect is schematically illustrated step-by-step in Figure 4-4. In the next sections, a detailed description of the fabrication process for each mask process will be described.

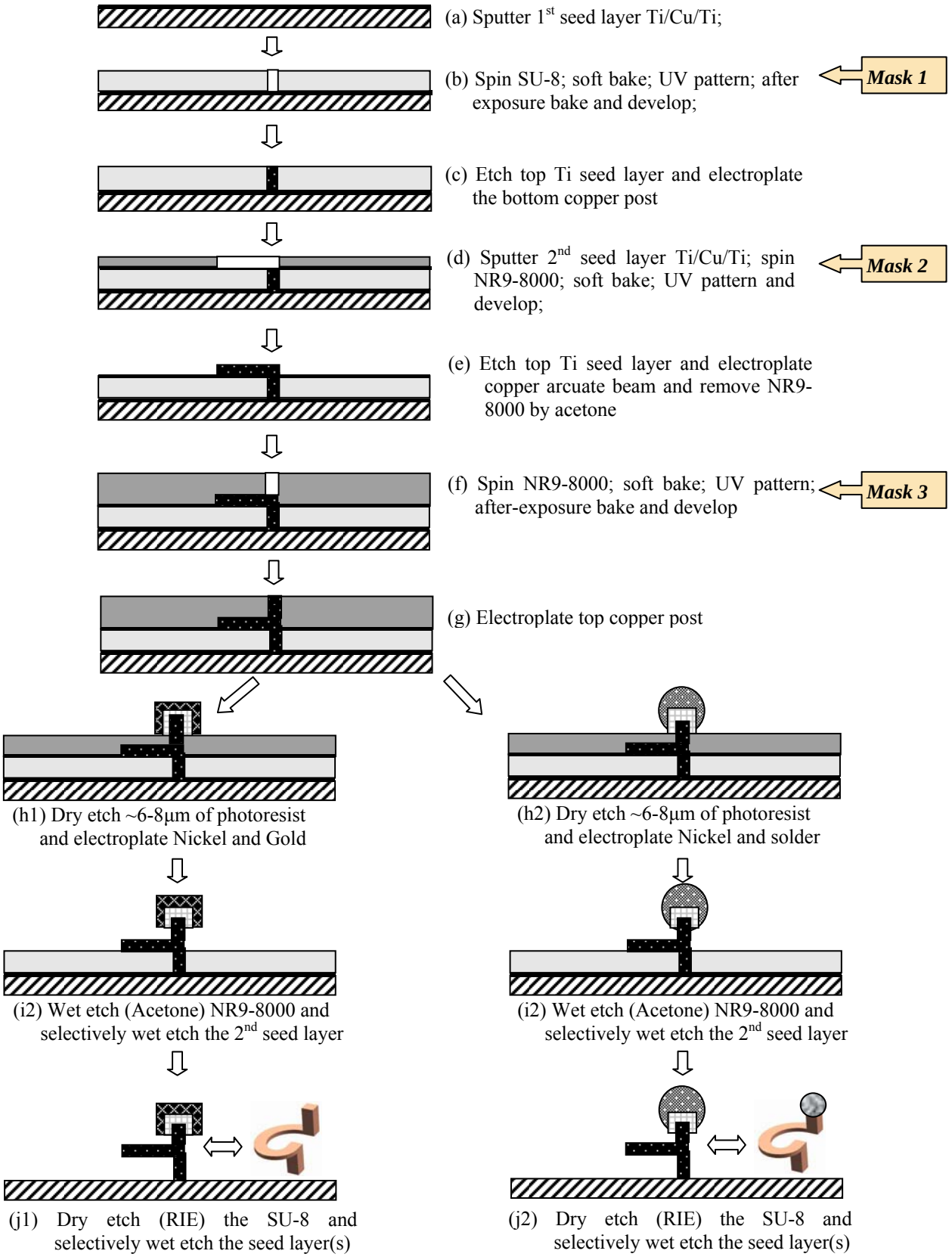


Figure 4-4: Fabrication Process of G-Helix Interconnect

4.4.1. Mask 1: Fabrication of Bottom Post

Mask 1 comprises of steps (a) to step (c) in Figure 4-4. In preparation for step (a), the wafer is first cleaned with acetone, methanol, isoproponol, and deionized (DI) water (in this order) to remove any contaminants that may be present on the surface of the wafer. The wafer is dried using nitrogen (N_2) gas and placed into a 95°C oven for 10 minutes to fully dehydrate the wafer.

After drying the wafer, the exposed copper pads are dipped in 10% sulfuric acid for 30 seconds to remove the oxide layer prior to sputtering the seed layer. Next, the dried wafer is placed in the unifilm sputter equipment to deposit of 300 $\overset{o}{A}$ titanium (Ti), 1000 $\overset{o}{A}$ copper (Cu) and 300 $\overset{o}{A}$ Ti. The layers of titanium are used for adhesion purposes where the first layer provides a strong adhesion between BCB and the sputtered copper, and the top titanium layer provides strong adhesion between copper and the thick photoresist that will be spun on and prevents oxidation of the copper seed layer. The copper is sputtered on to provide a continuous current flow and also acts as an ideal base material to grow the polycrystalline copper through electroplating [Seah 1998]. It should also be noted that it is crucial to utilize sputter equipment that has a low pump-down time to minimize oxide growth on the copper. Therefore, it is ideal to use the unifilm because it takes less than one minute to evacuate the air in chamber and have it under vacuum.

After sputtering the seed layer, the wafer is cleaned with acetone, methanol, isoproponol, and deionized (DI) water (in this order) and dehydrated in the oven. For the first layer, SU-8/25 is the photoresist used. The percent of solid determines the photoresist thickness versus the spin speed behavior. The process to spin and define the

features on SU-8 photoresist is as follows: spin coat, soft bake, expose, post expose bake (PEB) and develop.

Spin Coating

The spinning condition to achieve 38μm thickness goes as follows:

(1) Static Dispense: Approximately 1ml of SU-8 per inch of substrate diameter.

(2) Spread Cycle: Ramp to 500 rpm at 100 rpm/second acceleration and hold for 10 seconds.

(3) Spin Cycle: Ramp to 1750 rpm at an acceleration of 300 rpm/second and hold for a total of 30 seconds.

If air bubbles are present on the substrate, preheating the SU-8 that is to be dispensed to 60°C to reduce the viscosity of the SU-8 and allows the bubbles to rise to the surface and subsequently extinguish them from appearing.

Soft Bake

Once the photoresist has been applied to the substrate, it is soft baked to evaporate the solvent and densify the film. To reduce the edge bead around the outside edge of the wafer and remove the air bubbles entrapped in the photoresist, heating the SU-8 above the glass transition temperature, T_g, ($T_g \approx 55$°C for unexposed SU-8) is done. Convection oven could also be used to soft bake the photoresist, but SU-8 is normally done on a hot plate using a two plate contact hot plate process. The two plate contact hot plate process comprises of using two hot plates that are set at two different temperatures for soft baking. Table 4-1 provides the amount of time that the substrate is soft baked.

Table 4-1: Soft Bake Parameters for SU-8 38µm recipe.

Temperature (°C)	Soft Bake Time (Minutes)
65	5
95	15

During the initial soft baking at 65°C the solvent within the photoresist evaporates out of the film, to improve the coating fidelity, reduced edge beads, adhesion to substrate, and bubbles within the film. However, if the soft bake time is too long (especially for low aspect ratio structures), it is often desirable to work with photoresist with a bit more solvent because it speeds up the development time because it allows the film to be easier to strip. The substrate is allowed to cool back to room temperature before moving to the next processing step.

Expose

After soft baking the photoresist, the wafer is placed into a mask aligner for exposure. SU-8 is transparent and insensitive above 400nm but has high actinic absorption below 350nm. This can be seen in Figure 4-5.

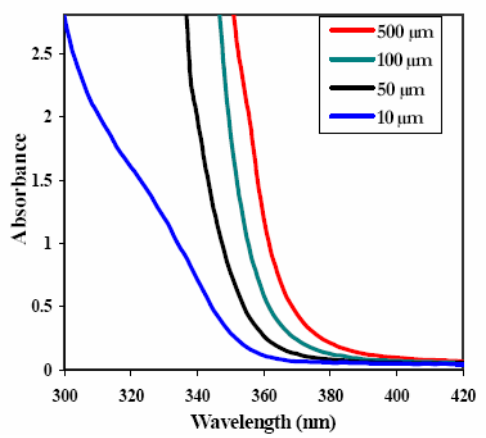


Figure 4-5: Absorbance vs. Wavelength for SU-8 [MicroChem 2004].

A Karl Suss MA-6 mask aligner is used for the exposure of the SU-8. Since the MA-6 used in the cleanroom is optimized for g-line applications, a filter that prevents wavelengths <360nm from being absorbed into the photoresist is used. This prevents over exposure of the top portion of the photoresist which would cause exaggerated negative sidewall profiles (also known as T-topping). To provide the best resolution, hard contact is used which holds the wafer against the mask while nitrogen is used to apply pressure to the bottom of the wafer.

The optimal exposure dosage is dependent on the film thickness and with the equipment used. A calibration was performed on the Karl Suss to determine the proper exposure dosage. It was determined that the recommended exposure dose is 110 mJ/cm^2. This value is based off of the source intensity and exposure time. For the 38μm recipe, for a 3.6mW/cm^2 (Measurement w/ 360nm filter), the exposure time would be around 30 seconds.

Post Exposure Bake (PEB)

In PEB, it is performed to selectively cross-link the exposed portions of the film. Precise control of PEB is critical in determining the subsequent development time. Table 4-2 provides the PEB parameters for the 38μm recipe.

Table 4-2: PEB Parameters for SU-8 38μm recipe.

Temperature (^oC)	Soft Bake Time (Minutes)
65	1
95	4

PEB baking is desired because the reactions initiated during exposure might not have run to completion. Adjusting the amount of exposure and PEB process conditions can control the amount of cross linking. Once the PEB is completed, there maybe cracking that occurs after PEB which is due to the following:

(1) Insufficent exposure dose.

(2) Shrinkage of the SU-8 as there is a CTE mismatch between the photoresist and silicon ($\alpha_{SU\text{-}8} \approx 52$ ppm/^{o}C).

To minimize the cracking in the SU-8 photoresist, ramping up to the PEB temperature and cooling it down at a controlled rate will minimize the stress induced to the photoresist.

Development, De-scum, and Etching

To expose the area that defines the bottom post, developing the area that was not exposed to UV light is performed in this process step. MicroChem® SU-8 developer is used. Since the feature consists of fairly high aspect ratio posts (Aspect ratio ~ 2.5:1), strong agitation is needed to produce good results. The substrate with the developer solution is immersed into an ultrasonic bath to clear out the deep trenches. The develop time used for the 38μm recipe is 2.5 – 3 minutes. Following development, the substrate is taken out and dried with a N_2 air. Water is not used to rinse the substrate as it does not produce positive results because a white residue is left on the surface of the photoresist.

After developing the photoresist, negative resist has a tendency to leave a thin polymer film at the resist/Ti interface. Therefore a mild dry-etch process, also called de-scumming, removes this unwanted resist left behind. This also enhances the adhesion

between the electroplated structure and the substrate. The recipe used to dry etch SU-8 in the RIE is as follows where SCCM stands for standard cm^3/min:

- RF Power: 250W
- Chamber Pressure: 300mTorr
- O_2 Flow Rate: 50 SCCM
- CHF_3 Flow Rate: 7 SCCM

The substrate is de-scummed in the RIE for approximately two minutes as the etch rate for the recipe above is ~0.5 μm/min.

Next the top Ti seed layer is etched away using Buffered Oxide Etch (BOE), 6:1 HF: NH_4F. The substrate is dipped in water to prevent air bubbles from forming when the substrate is dipped into the BOE solution. Therefore, the etching is isotropic throughout the wafer. The etch rate is relatively slow (~100Å/sec) and the etching is complete when a light brown color of copper appears. The etching process approximately one minute to complete. Once this can be seen, the substrate is removed from the BOE solution and rinsed with DI water for two minutes. Carefully monitoring the BOE etching will minimize etching of the Ti that is under the photoresist which is referred to as 'undercutting'.

Electroplating

After the SU-8 photoresist has defined the base post, the next step in the process flow is to fabricate the base post of the compliant interconnect. The fabricated comprises of an electroplating process. There are four main components to an electroplating bath which are: cathode, anode, current source and plating solution. A typical setup of a copper electroplating bath is shown in Figure 4-6.

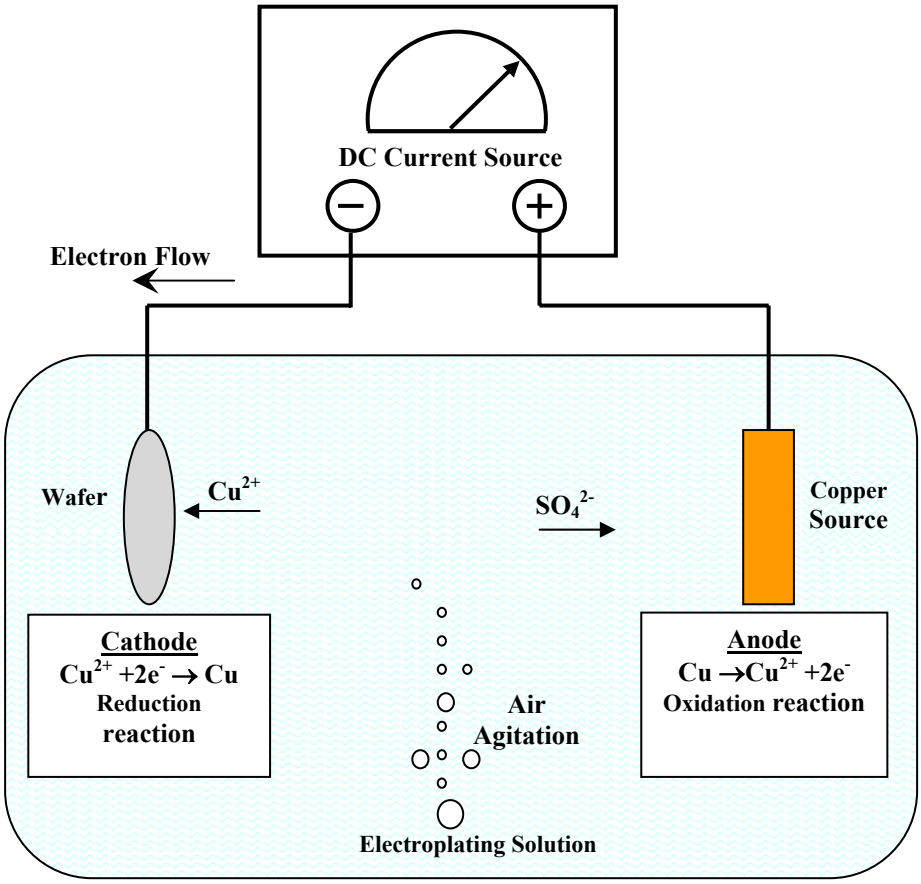


Figure 4-6: Copper Electroplating Setup [Zhu 2003].

The theory behind electroplating consists of a power source connected in series with the anode and cathode. Where the cathode is the wafer on which metal is to be deposited. The anode is a metal that does not react with the electroplating solution which is typically a metal foil or an electrically conducting wire. With regards to a copper plating solution, the copper ions from the solution are deposited onto the surface of the wafer due to the reduction reaction that occurs. At the anode side, oxidation of the copper metal generates copper ions which will be transferred through the bath onto the wafer. To agitate the system, a stirrer or pump that provides ample flow through the system is used to provide good uniformity through the system.

A conventional high acidic copper plating solution is used to electroplate the features of the G-Helix. The recipe for the bath goes as follows:

- $CuSO_4$ – 73 g/l
- H_2SO_4 – 210 g/l
- $CuCl_2$ – 67 mg/l
- H_2O – Fill up to the 1L mark

Figure 4-7 displays the surface morphology of the electroplated copper for a current density of 5.33 mA/cm^2.

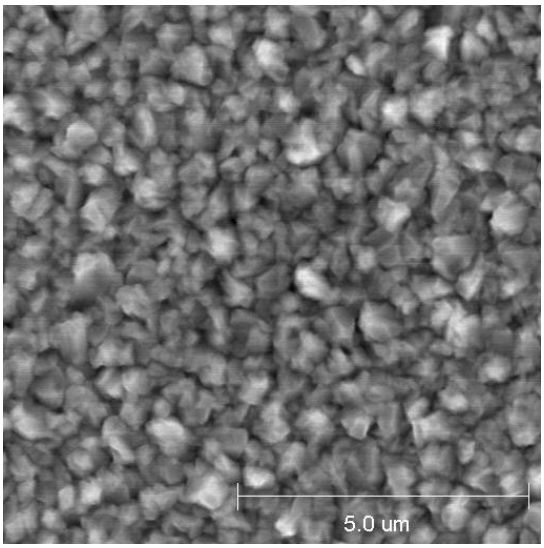


Figure 4-7: Surface Morphology of Copper for Current Density of 5.33 mA/cm^2.

Industry standard for electroplating is 30 Amps per Square Feet (ASF). In electroplating the first mask structure, the total area of copper that is electroplated is approximately 2 cm^2. Therefore, a current of 60mA is used which equates to 30 mA/cm^2 (~28ASF) is used to electroplate the base post at 500 rpm stirring rate of the solution.

The surface morphology for copper plated at 30 mA/cm^2 is similar to what is seen at 5.33 mA/cm^2. At 30 mA/cm^2, the plating rate for copper is approximately 0.5μm/min.

To avoid overplating, the wafer is taken out and inspected periodically with a profilometer and microscope. Prior to placing the wafer back into the solution, the copper is dipped in 10% sulfuric acid for 30 seconds and rinsed with DI water for one minute. If this is not done, the thin oxide layer will provide poor adhesion between the post and subsequent copper that is electroplated on top of the oxide layer. Figure 4-8 displays an example of the poor adhesion when the wafer was pulled out for inspection and not dipped in 10% sulfuric acid prior to additional electroplating.

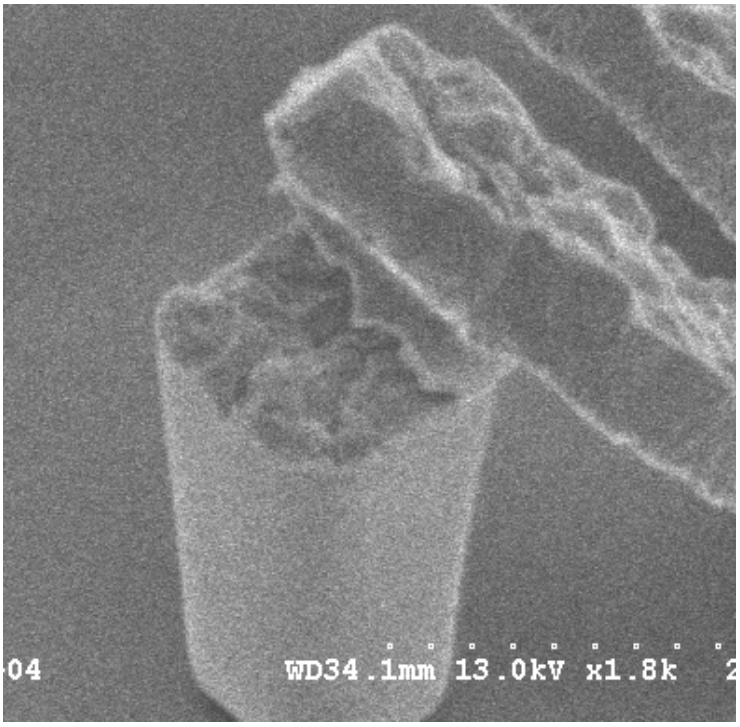


Figure 4-8: Failure due to poor adhesion between bottom post and subsequent electroplated copper.

After electroplating the substrate is displayed in Figure 4-9.

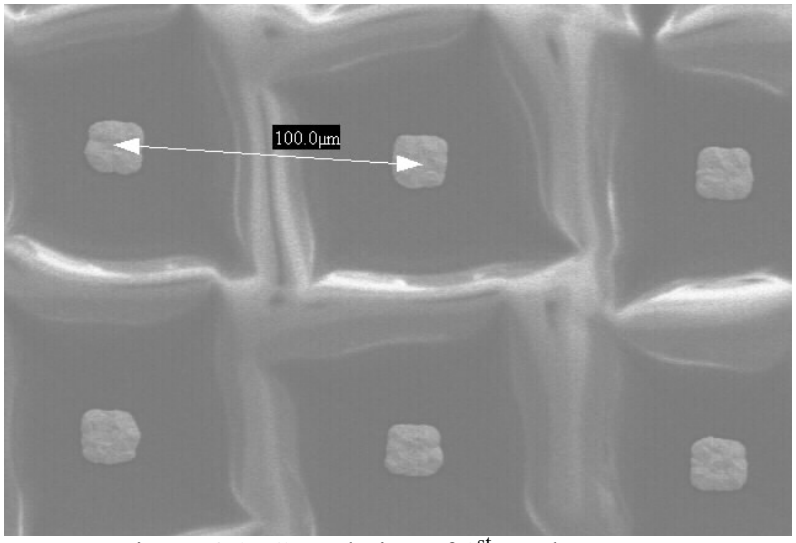


Figure 4-9: Completion of 1st mask process.

4.4.2. Mask 2: Fabrication of Arcuate Beam

Mask 2 comprises of steps (d) to step (e) in Figure 4-4. In preparation for step (d), the wafer is again cleaned with acetone, methanol, isoproponol, and deionized (DI) water (in this order) to remove any contaminants that may be present on the surface of the wafer. The wafer is dried using nitrogen (N_2) gas and placed into a 95°C oven for 10 minutes to fully dehydrate the wafer.

After drying the wafer, the exposed copper pads are dipped in 10% sulfuric acid for 30 seconds and rinsed in DI water for one minute to remove the oxide layer prior to sputtering the seed layer. Next, the dried wafer is placed in the unifilm sputter equipment to deposit of 300 $\overset{o}{A}$ titanium (Ti), 1000 $\overset{o}{A}$ copper (Cu) and 300 $\overset{o}{A}$ Ti for the same reasons as was stated in Section 4.4.1. Again, it should also be noted that it is crucial to utilize sputter equipment that has a low pump-down time to minimize oxide growth on the copper. Therefore, it is ideal to use the unifilm because it takes less than one minute to evacuate the air in chamber and have it under vacuum. Figure 4-8 displays an example of good adhesion between the interface of the first mask and second mask process. Failure was because the wafer was not dipped in 10% sulfuric acid to remove any excess oxides that were built up during routine inspection of the electroplating of the 1st mask process.

After sputtering the seed layer, the wafer is cleaned with acetone, methanol, isoproponol, and deionized (DI) water (in this order) and dehydrated in the oven. For the second layer, Futurrex NR9-8000 photoresist used. The process to spin and define the features on NR9-8000 photoresist is as follows: spin coat, soft bake, expose, post expose bake (PEB) and develop.

Spin Coating

The spinning condition to achieve 8μm thickness goes as follows:

(1) Static Dispense: Approximately 1ml of NR9-8000 per inch of substrate diameter.

(3) Spin Cycle: Ramp to 3000 rpm at an acceleration of 1000 rpm/second and hold for a total of 30 seconds.

Soft Bake

Once the photoresist has been applied to the wafer, it is soft baked by a two plate contact hot plate process. Table 4-3 provides the amount of time that the substrate is soft baked.

Table 4-3: Soft Bake Parameters for NR9-8000 8μm recipe.

Temperature (^{o}C)	Soft Bake Time (Minutes)
70	5
110	4

Expose

After soft baking the photoresist, the wafer is placed into a mask aligner for exposure. An EV620 mask aligner is used for the exposure of the NR9-8000. This equipment is optimized for i-line applications. To provide the best resolution, hard contact is used.

The optimal exposure dosage is dependent on the film thickness and with the equipment used. A calibration was performed on the EV620 to determine the proper

exposure dosage. It was determined that the recommended exposure dose is 210 mJ/cm^2. This value is based off of the source intensity and exposure time. For the 8μm recipe, for an 11 mW/cm^2, the exposure time would be 20 seconds.

Post Exposure Bake (PEB)

In PEB, it is performed to selectively cross-link the exposed portions of the film. Table 4-4 provides the PEB parameters for the 8μm recipe.

Table 4-4: PEB Parameters for NR9-8000 8μm recipe.

Temperature (^{o}C)	Soft Bake Time (Minutes)
70	3

Development, De-scum, Etching, and Electroplating

To expose the area that defines the arcuate beam, Futurrex RD6 developer is used. Light agitation is needed to produce good results. The develop time used for the 8μm recipe is 40 seconds. Following development, the wafer is taken out and rinsed in water and dried with a N_2 air.

After developing the photoresist, de-scumming is done to remove and residual photoresist that was left behind after development. The recipe used in the RIE for dry etching NR9-8000 is as follows:

- RF Power: 300W
- Chamber Pressure: 280mTorr
- O_2 Flow Rate: 45 SCCM
- CHF_3 Flow Rate: 5 SCCM

The wafer is dry-scummed in the RIE for approximately two minutes as the etch rate for the recipe above is ~0.5 μm/min.

Next the top Ti seed layer is etched away using Buffered Oxide Etch (BOE), 6:1 HF: NH_4F. The wafer is dipped in water to prevent air bubbles from forming when the wafer is dipped into the BOE solution. The etch rate is relatively slow (~100Å/sec) and the etching is complete when a light brown color of copper appears. The etching process approximately one minute to complete. Once this can be seen, the wafer is removed from the BOE solution and rinsed with DI water for two minutes. Carefully monitoring the BOE etching will minimize undercutting.

With the exposed copper, it needs to be prepared for electroplating. Before electroplating, the wafer is dipped into 10% sulfuric acid for 30 seconds and rinsed in DI water for one minute. The exposed area was calculated to be ~2 cm^2 and with a current density of 30 mA/cm^2, it takes approximately 20 minutes to electroplate 8μm. After electroplating is completed, the NR9-8000 is removed with acetone.

4.4.3. Mask 3A: Fabrication of Top Post Without Solder

Mask 3A comprises of steps (f) to step (j1) in Figure 4-4. In preparation for step (f), the wafer is again cleaned with acetone, methanol, isoproponol, and deionized (DI) water (in this order) to remove any contaminants that may be present on the surface of the wafer. The wafer is dried using nitrogen (N_2) gas and placed into a 95°C oven for 10 minutes.

After drying the wafer, Futurrex NR9-8000 photoresist is prepared is applied onto the wafer. Seed layers do not need to be applied as the copper arcuate beam area is large enough to be used as a seed layer to electroplate the top post. The steps to spin and

define the features on NR9-8000 photoresist are the same as Section 4.4.2, but the process values are different for the 42µm recipe. A 42µm is used to produce the features because since we etched away the photoresist to fabricate the second layer, the photoresist that is spun for the 3rd mask structure needs to compensate for the height of the 2nd mask structure.

Spin Coating

The spinning condition to achieve 8µm thickness goes as follows:

(1) Static Dispense: Approximately 1ml of NR9-8000 per inch of wafer diameter.

(3) Spin Cycle: Ramp to 600 rpm at an acceleration of 500 rpm/second and hold for a total of 60 seconds.

Soft Bake

Once the photoresist has been applied to the wafer, it is soft baked by a two plate contact hot plate process. Table 4-5 provides the amount of time that the wafer is soft baked.

Table 4-5: Soft Bake Parameters for NR9-8000 42µm recipe.

Temperature (^{o}C)	Soft Bake Time (Minutes)
70	5
110	10

Expose

After soft baking the photoresist, the wafer is placed into a mask aligner for exposure. An EV620 mask aligner is used for the exposure of the NR9-8000. This

equipment is optimized for i-line applications. To provide the best resolution, hard contact is used which holds the wafer against the mask while nitrogen is used to apply pressure to the bottom of the wafer.

The optimal exposure dosage is dependent on the film thickness and with the equipment used. A calibration was performed on the EV620 to determine the proper exposure dosage. It was determined that the recommended exposure dose is 210 mJ/cm^2. This value is based off of the source intensity and exposure time. For the 42μm recipe, for an 11 mW/cm^2 (Measurement w/ 360nm filter), the exposure time would be around 65 seconds.

Post Exposure Bake (PEB)

Table 4-6 provides the PEB parameters for the 42μm recipe.

Table 4-6: PEB Parameters for NR9-8000 42μm recipe.

Temperature (^oC)	Soft Bake Time (Minutes)
70	5

Development, De-scum, Etching, and Electroplating

To expose the area that defines the top post, Futurrex RD6 developer is used. Light agitation is needed to produce good results. The develop time used for the 42μm recipe is two minutes. Following development, the wafer is taken out and rinsed in water and dried with a N_2 air.

After developing the photoresist, de-scumming is done to remove and residual photoresist that was left behind after development. The recipe used in the RIE for dry etching NR9-8000 is as described in the Development, De-Scum, and Etching Section

4.4.2. The wafer is dry-scummed in the RIE for approximately two minutes as the etch rate for the recipe above is ~0.5 μm/min.

With the exposed copper, it needs to be prepared for electroplating. Before electroplating, the wafer is dipped into 10% sulfuric acid for 30 seconds and rinsed in DI water for one minute. The exposed area was calculated to be 0.1 cm^2 and with a current density of 30 mA/cm^2, it takes approximately 40 minutes to electroplate 42μm.

Under Bump Metallization (UBM) Application

To prepare the G-Helix for assembly onto an organic substrate, the top post needs to have an UBM to provide a barrier layer and antioxidation barrier between copper and the solder. The structure of the UBM used for the G-Helix comprises of Nickel (Ni) and Gold (Au). Nickel is used as the UBM because it acts as a barrier layer by preventing diffusion of metal species and ionic contaminants into the G-Helix. If a barrier layer is not present brittle intermetallics would form thus decreasing the reliability of the interconnect. With regards to gold, it is an antioxidation barrier to prevent oxides from forming on the Nickel. This layer need not be too thick in order to not embrittle the UBM-solder bump interface due to the formation of intermetallics. For example, if lead-tin solder is used to assemble the G-Helix, the gold will rapidly dissolve in the liquid tin, forming brittle tin-gold intermetallics minimizing the reliability of the interconnection.

When the G-Helix is fabricated without solder electroplated, it is expected that during assembly the top post will be embedded into solder that is either screen-printed or electroplated on the board side. Therefore, a portion of the top post will need a barrier layer to prevent solder from diffusing into the top post. To form a barrier layer on the top post of the G-Helix, no additional masks are needed to define and electroplate the solder.

Instead, the photoresist used to define the top post is 'back etched' in the RIE to expose 5 – 8 μm of the side walls. The dry etch recipe used is the one described earlier for NR9-8000. Once the photoresist is 'back etched', the wafer is immersed in 10% sulfuric acid for 30 seconds and rinsed in DI water. Next, nickel is electroplated onto the exposed copper post using a commercially available bath from Technics Inc. The current density was 30mA/cm^2 and stirring rate of 500 rpm of the solution, and approximately 2 – 3μm is electroplated which takes approximately 30 minutes. Next, <1μm of gold is electroplated using a commercially available bath from Technics Inc. At a current density of 30mA/cm^2 at 500 rpm stirring rate of the solution, it takes approximately 30 minutes to electroplate the gold. Figure 4-10 displays the completed UBM process that was discussed.

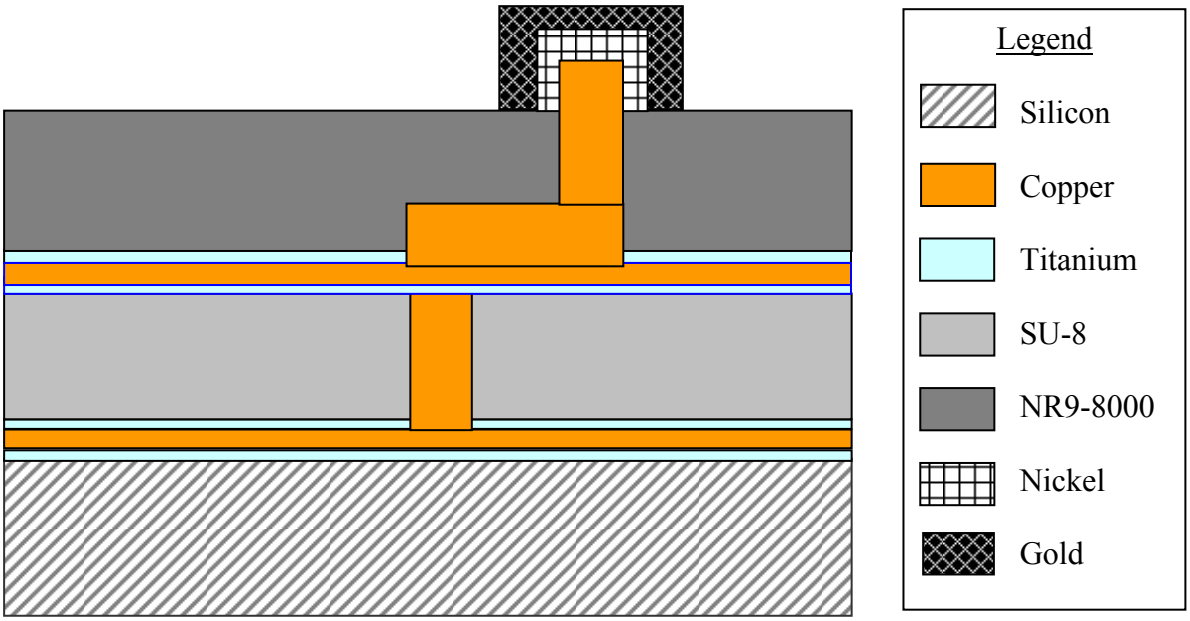


Figure 4-10: Fabrication of UBM Barrier Layer on Top Post.

Structure Releasing

Once all the features of the G-Helix and UBM have been fabricated, the dies are subsequently singulated into individual dies. The photoresist is left on during the dicing process to prevent any damage during the dicing process as high pressure water is sprayed on to the surface of the wafer. With the individual dies, the seed layers and photoresist is removed using a "top-down" process. First the NR9-8000 is removed with Acetone. Next the seed layers are removed where the titanium seed layer is removed with BOE. This takes approximately one minute to complete. Next the copper seed layer is selectively etched. This needs to be done very carefully as to minimize the etching of the G-Helix. There are a variety of chemical combinations that can be used to etch copper. However, the chemical etchant should be chosen which selectively etches copper exclusively and not the UBM that was electroplated on the top post. Therefore, Aluminum Enchant Type D supplied by Transene works very well in selectively etching copper exclusively. The etching takes approximately one minute, and after etching the copper, it is dipped in DI water for two minutes. Next the wafer is dipped into BOE to remove the bottom titanium layer for one minute and then dipped into water for two minutes. This releases the second and third mask features.

Next the base SU-8 layer is removed using RIE. The recipe used was described in Section 4.4.1. The dry etch rate is 0.5μm/minute so it takes approximately 74 minutes to remove the SU-8. Once this is completed, the seed layers of Ti/Cu/Ti is removed using the same etch process as described in the previous paragraph.

Fabrication Results

Micrographs were taken of the free-standing structure at 100μm pitch. Figure 4-11 displays a global isometric view of the peripheral arrayed G-Helix interconnects.

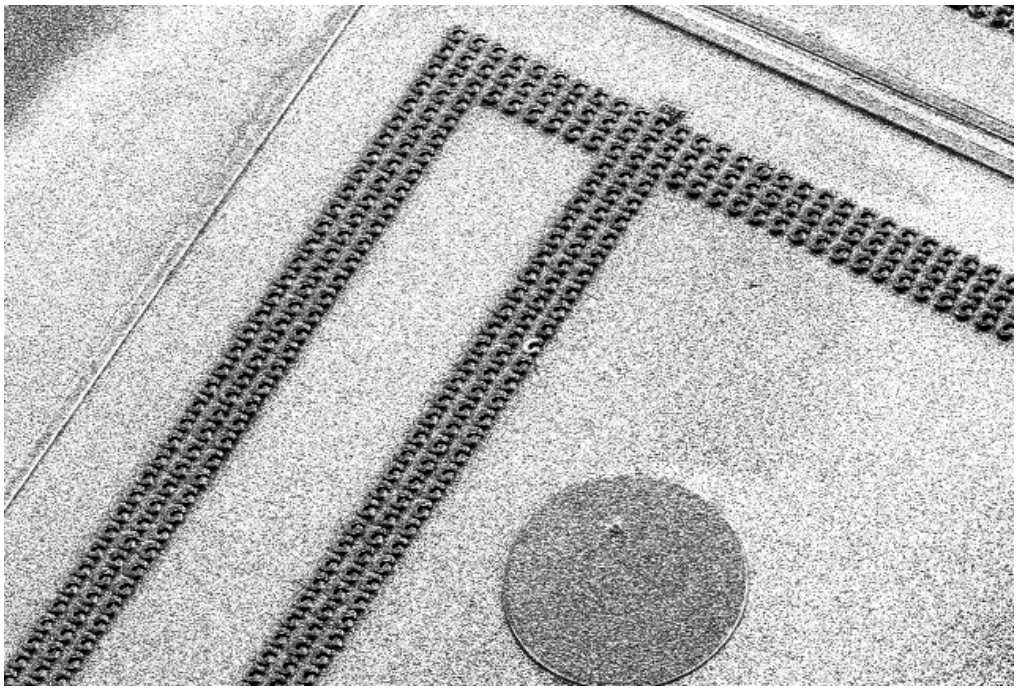


Figure 4-11: Global Isometric View of G-Helix

Figure 4-12 displays additional close-up images of the free-standing G-Helix interconnects.

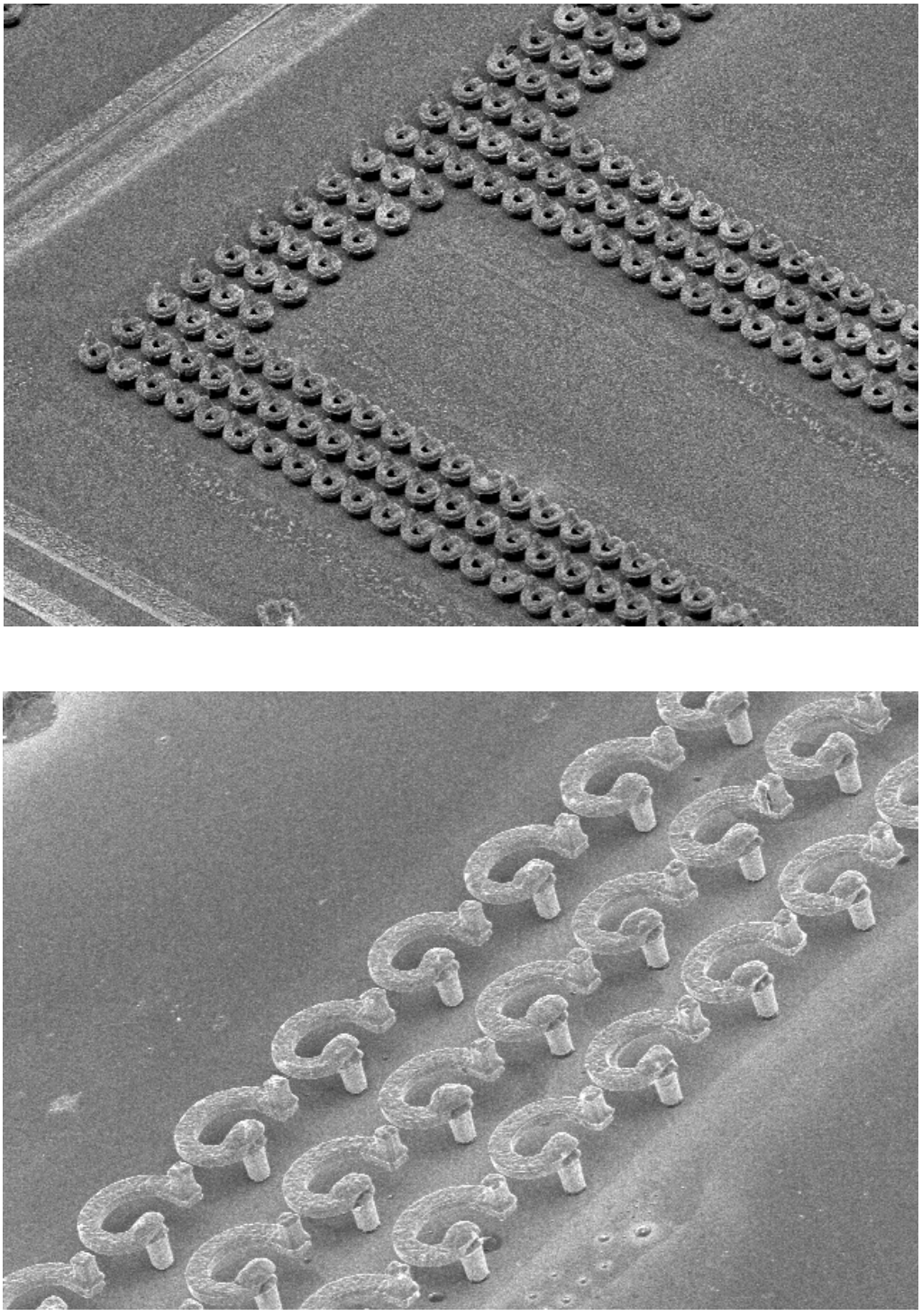


Figure 4-12: Micrographs of 100μm pitch G-Helix.

Figure 4-13 provides a close-up image of a single G-Helix interconnect.

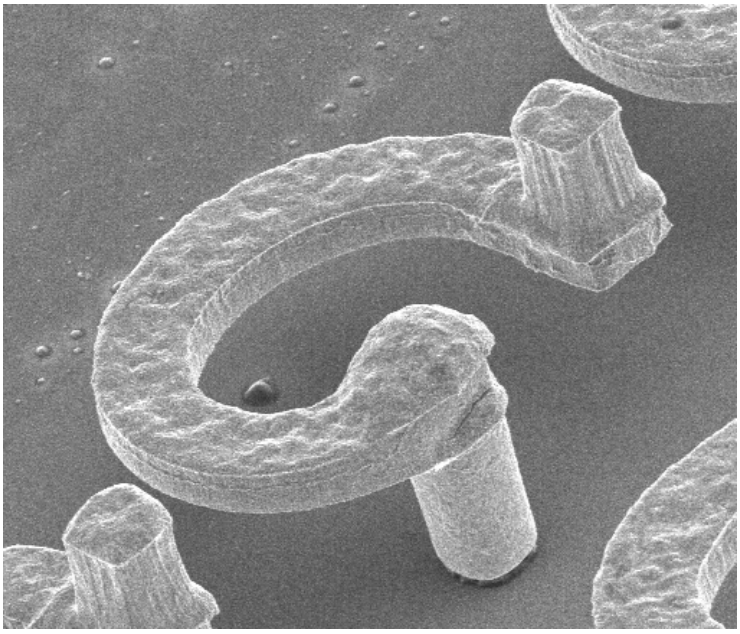


Figure 4-13: Micrograph of a Single Free-Standing G-Helix.

4.4.4. Mask 3B: Fabrication of Top Post With 60Sn/40Pb Solder

After the top post has been fabricated for the third mask process, the second methodology for the fabrication of the interconnect is electroplating solder onto the end post which comprises of steps (h2) – (j2). Figure 4-14 displays the fabrication process with solder.

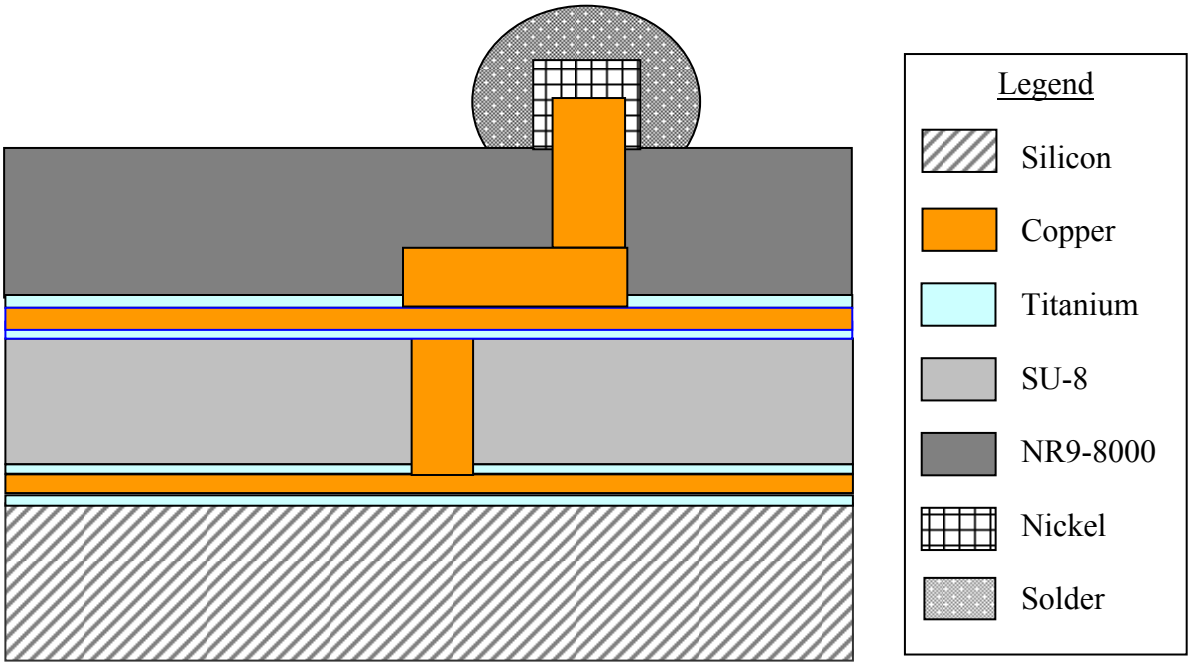


Figure 4-14: Fabrication of UBM Barrier Layer and Solder on Top Post

As seen in Figure 4-14 the difference the UBM here is that gold is not electroplated on to the end post prior to electroplating the solder. Gold is used to prevent oxidation of the nickel so that when the G-Helix is interconnected to solder on the board side, the interconnection is good. However, since solder is electroplated on the G-Helix, prior to the solder electroplating, the wafer is immersed in 10% sulfuric acid 30 seconds

and rinsed in DI water. Therefore, the sulfuric acid dip removes the layer of oxide that the layer of electroplated gold would have prevented.

To electroplate solder, any type of leaded of lead-free solder can be incorporated. In this work, 60Sn/40Pb solder is used. The leaded solder plating solution is commercially available by Technics Inc. (NF820 HS 60/40) where a current density of 30 mA/cm^2 and stirring rate of 500 rpm of the solution is used. The electroplating takes approximately 130 minutes to plate a solder ball with an in-plane diameter of 35μm. As mentioned in Section 4.4.3 on structure releasing, the process is the same to produce the free-standing structure.

Fabrication Results

Micrographs were taken of the free-standing structure with 60Sn/40Pb solder at 100μm pitch. Figure 4-15 displays some images of the free-standing G-Helix interconnects with electroplated 60Sn/40Pb solder.

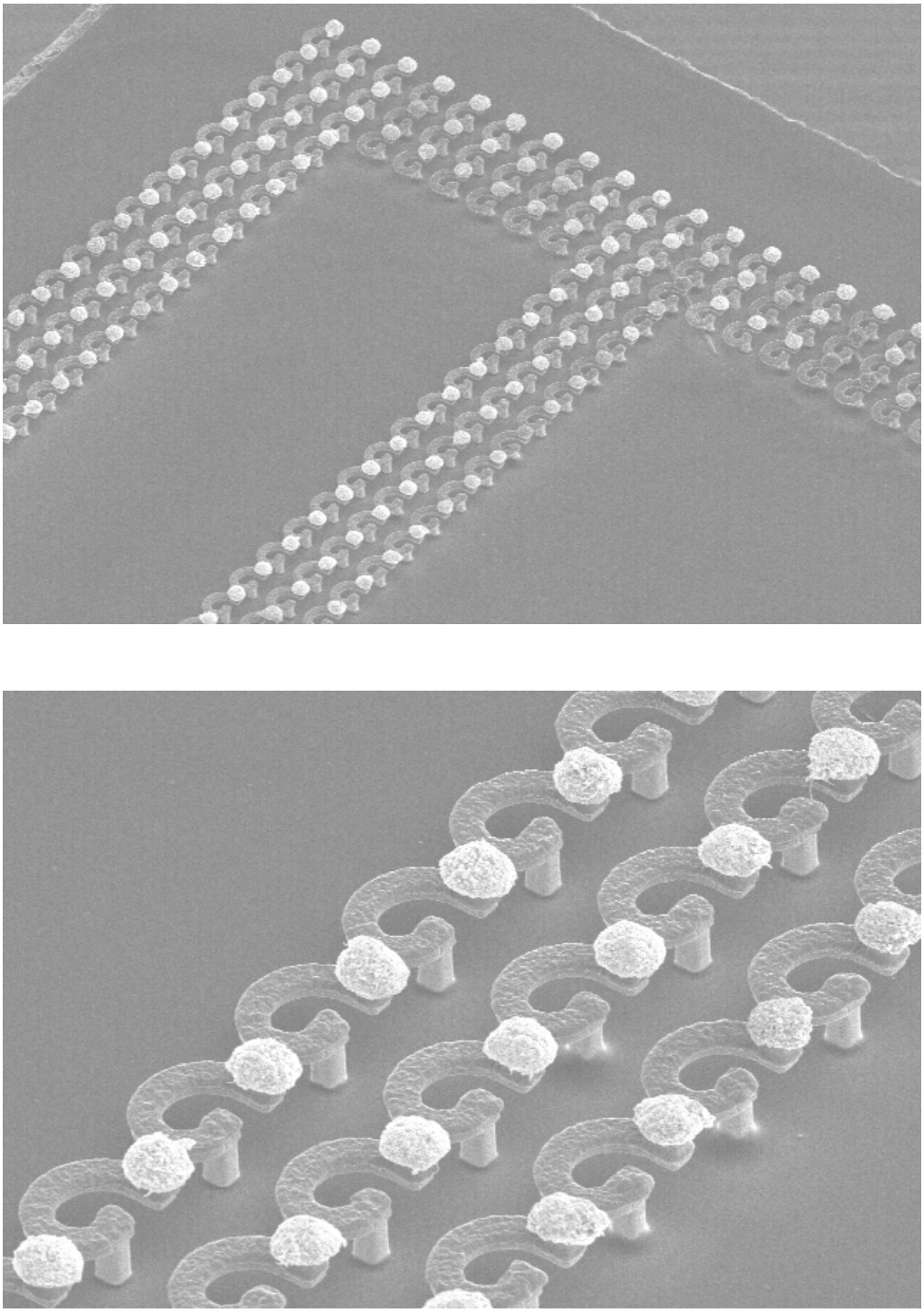


Figure 4-15: Micrographs of 100μm pitch G-Helix With 60Sn/40Pb.

Figure 4-16 provides a close-up image of a single G-Helix interconnect with 60Sn/40Pb solder.

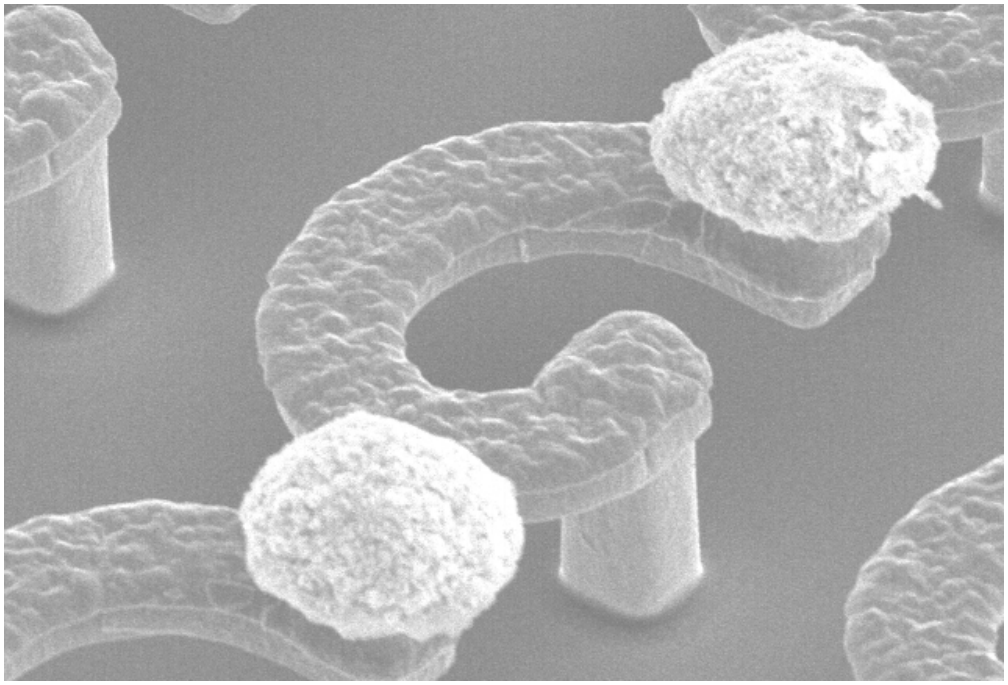


Figure 4-16: Micrograph of a Single Free-Standing G-Helix with 60Sn/40Pb Solder.

4.5. Post-Fabrication Analysis

After fabrication of the interconnects was performed, post-fabrication analysis of the G-Helix was performed. The force vs. displacement was performed for the out-of-plane of the interconnect, and also the interconnect was excessively deformed to understand the ductility of the interconnect.

4.5.1. Force vs. Displacement

The out-of-plane compliance of the interconnect was characterized with the use of a nanoindenter. For fine pitch packages, good out-of-plane is desired to compensate for the non-planarity of substrate and to ensure a reliable contact during assembly and probing. Using a Mechanical Test System (MTS®), a small displacement was applied in the out-of-plane direction of the G-Helix and the relative force was obtained. Figure 4-17 displays the results from the test.

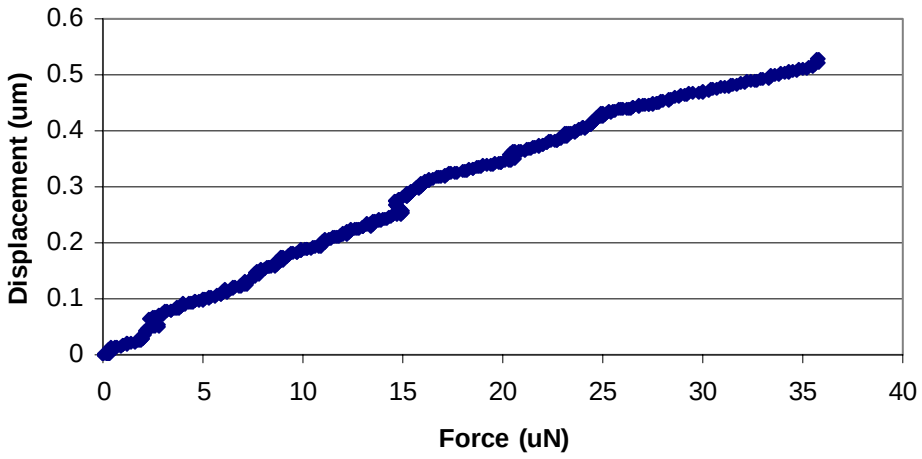


Figure 4-17: Force vs. Displacement in the Out-of-Plane Direction.

From Figure 4-17, the slope of the line is a measurement of the compliance of the G-Helix structure. Therefore, the slope was calculated to be 14.7mm/N. The out-of-plane compliance was compared to the other two methodologies which are RSM and FEM. Table 4-7 provides a comparison of the out-of-plane compliance based on the three methodologies.

Table 4-7: Comparison of the Compliance Obtained From Three Methodologies.

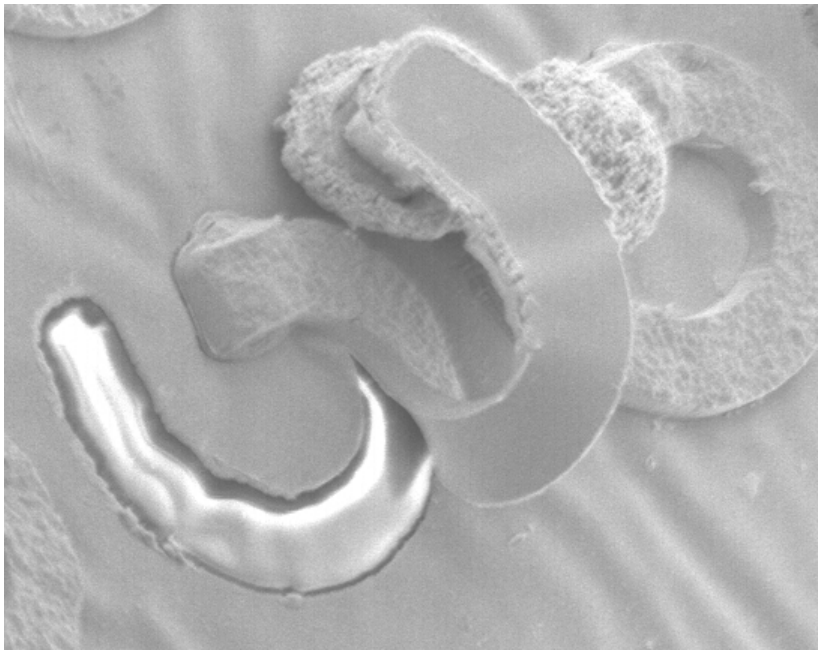
Compliance	RSM	FEM	Empirical
C_y (mm/N)	11.2	10.2	14.7

It is seen that the experimental values are close what was predicted by the numerical models. A reason for the difference between the values could be due to geometric variations from fabricating the interconnects. When producing the free-standing G-Helix structure, etchant is used to remove the copper seed layer, and this also

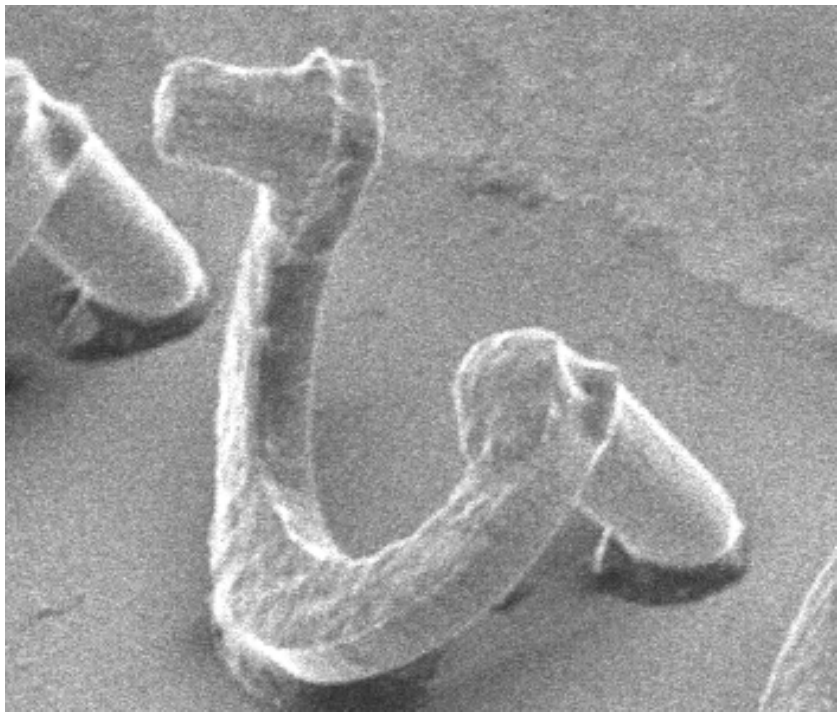
subsequently etches the copper interconnect structure slightly. Therefore, the geometry of the actual fabricated free-standing structure would vary from what was defined during the photolithography process.

4.6. Excessive Deformation of the G-Helix

To fabricate the G-Helix interconnects, copper was selected. Copper was chosen to electroplate the features of the G-Helix because of its low resistivity and electromigration stability characteristics. Also, copper is a very ductile material. Ductility is defined as the ability of a material to plastically deform without breaking or fracturing, with the cohesion between the molecules remaining sufficient to hold them together. In general, copper is considered a ductile material should be able exhibit large deformation before fracture. To exhibit the ductility of the G-Helix, it was excessively deformed as depicted in Figure 4-18.



(a) The Arcuate Beam Was Excessively Peeled Back.



(b) Freestanding G-Helix Was Excessively Displaced.

Figure 4-18: Examples of the Ductility of the Electroplated G-Helix Structure.

As can be seen from Figure 4-18, the electroplated copper used to fabricate the G-Helix is indeed ductile. When the arcuate beam was excessively bent, the structure did not exhibit brittle fracture. Instead, the interconnect plastically deformed. Also, when a free-standing structure was produced and excessively deformed as shown in Figure 4-18(b), the interconnect structure did not break. Another interesting observation that should be noted is the adhesion between the three mask layers and especially between the base post to the silicon substrate. When the free-standing is excessively deformed, the support at the interface to the silicon substrate and between mask structures is strong enough to provide a strong bond thus allowing the interconnect to deform.

CHAPTER 5

BOARD ASSEMBLY & RELIABILITY ASSESSMENT

In this chapter, the assembly methodology and reliability assessment of G-Helix will be discussed. The first section provides a description of the design of the test vehicle. The second section focuses on the methodology of assembly and results from assembly. The third section focuses on the reliability assessment of the assembly.

5.1. Board Layout

After the 20 x 20mm three-row peripheral-array 100μm pitch free-standing G-helix interconnects has been fabricated and singulated into individual dies, they are ready to be assembled onto a PWB. To PWB used to assemble the G-Helix onto is a high modulus low CTE (α_{FR-4} = 11 ppm/°C) FR-4 substrate. Figure 5-1 displays an image of the design of the test board to assess the electrical and thermo-mechanical reliability of the G-Helix.

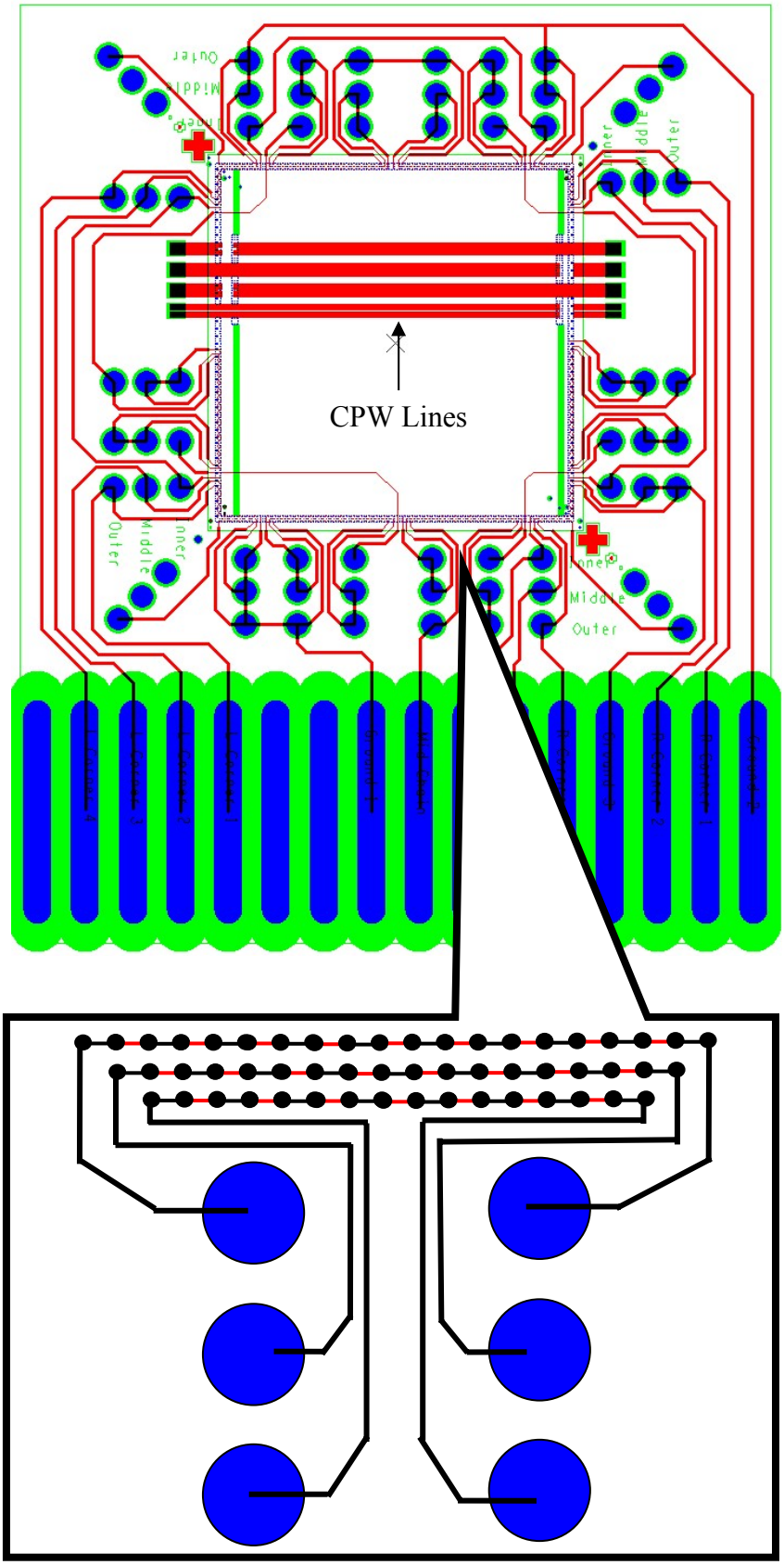


Figure 5-1: Electrical and Thermo-mechanical Reliability PWB.

The board is designed for both in-situ monitoring and manual probing the reliability of the interconnects. The three primary daisy chains designed onto the chip side are subdivided into ten channels on the PWB side to monitor the reliability of the interconnects around the die. The chains are broken up so that observations can be made on each row and sub-sections of the die exclusively. Probe pads are included around the peripheral of die so when a failure is observed, the location of the failure can be narrowed down. Also, Four Co-Planar Waveguides (CPW) lines are included in the design so as to understand the electrical parasitics of the interconnects and also understand the performance of the interconnect when a high frequency is propagated through the system.

5.1.1. CTE Mismatch

The combination of fine pitch and large die presents a unique assembly challenge in aligning the interconnects on the chip to the corresponding pads. When the assembly is heated up, the organic substrate will expand at a faster rate compared to the silicon die. Therefore, the corresponding copper pads that are supposed to be in line with each other, will be offset due to the thermal expansion. Due to this effect, to compensate for the expansion, the pads on the PWB are designed to minimize the offset. Figure 5-2 provides the dimensions of the silicon die used for the analysis.

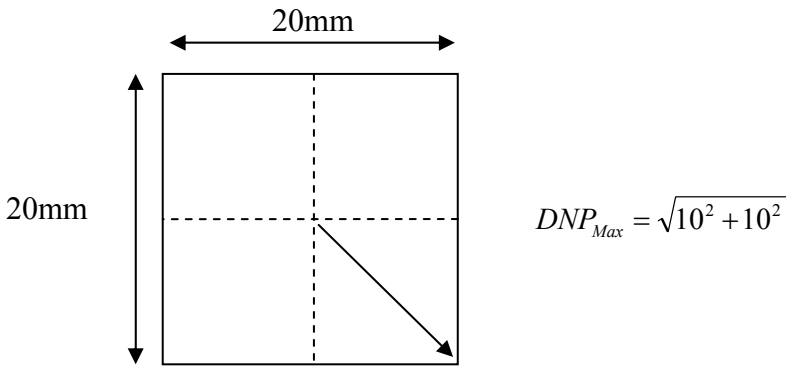


Figure 5-2: Die Dimensions

The maximum Distance from Neutral Point (DNP) is from the center to the outermost interconnect which is located at one of the four corners of the die which is ≈14mm. Assuming a differential CTE of 8ppm/°C between the chip and the board, and a ΔT of 175°C which is the difference from reflow (200°C) to room temperature (25°C), the maximum free-air displacement can be calculated as follows:

$$\Delta_{Max} = DNP_{Max} * \Delta\alpha_{Si-FR-4} * \Delta T_{\mathrm{Re}\,flow-Room\,Temp} \qquad 5\text{-}1$$

From Equation 5-1, the total differential free-expansion along the diagonal of the assembly for the given temperature change is calculated which turns out to be ≈20μm. At the pitch requirements set forth in this work, this will result in a significant mis-match between the corresponding copper landing pads of the silicon to the PWB, greatly reducing the reliability of the interconnection.

5.1.2. Reduced Pitch on the PWB

To accommodate for a portion of the expansion, the position of the pads on the organic board were redesigned so that the copper pad on the PWB will align with the

corresponding interconnect on the chip at 150°C. Therefore, this will limit the resultant misalignment to within 6μm.

The electrical and thermo-mechanical testbed utilized for this work is comprised of a peripheral arrayed die with a 190 x 190 depopulated outer row. Therefore, there are 191 copper pads for the outermost row which populates 19 x 19mm of the die. Figure 5-3 depicts the layout of the die.

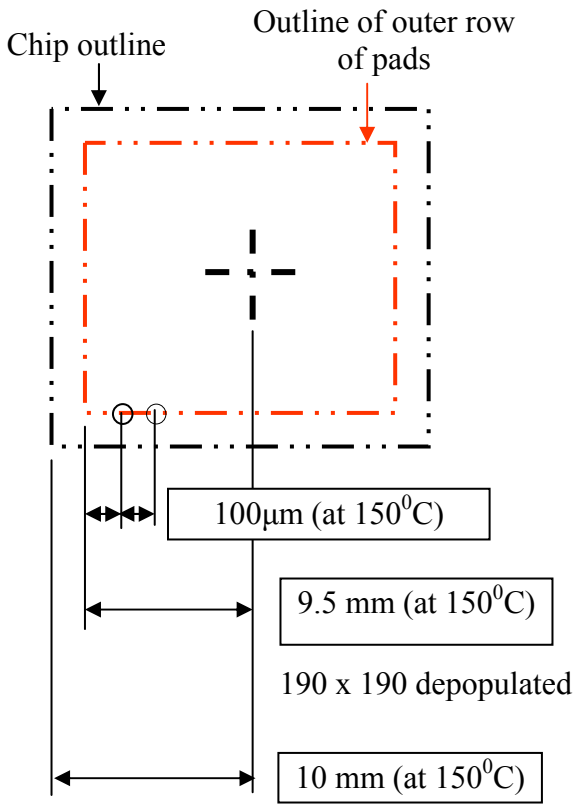
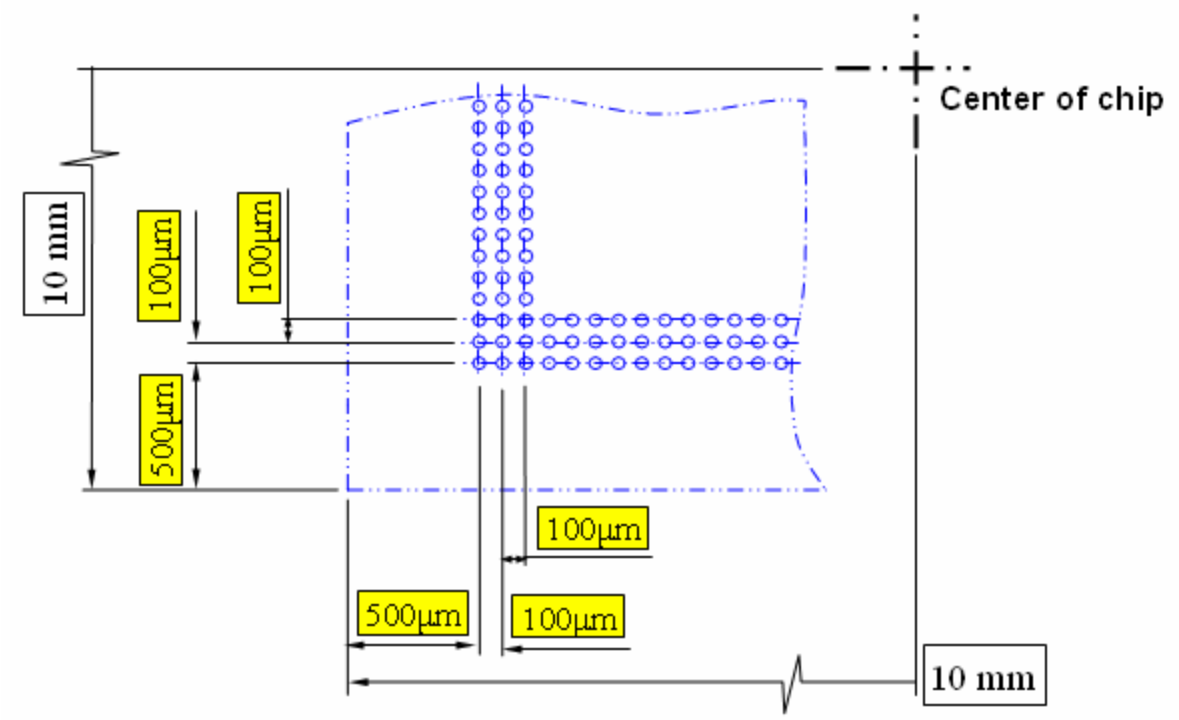


Figure 5-3: Layout of the Silicon Die.

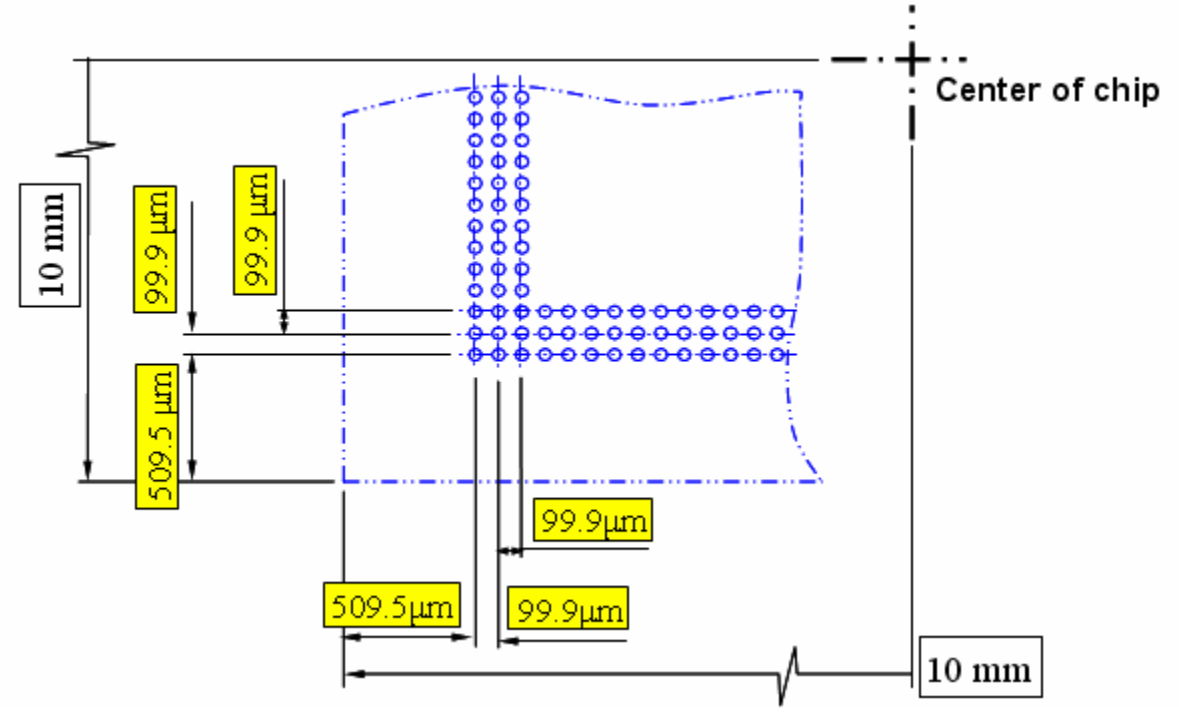
Since the PWB has a higher CTE, the pitch for the copper pads needs to be redefined. The calculation is based off of Equation 5-1, where the parameters are as follows:

- Differential CTE between the silicon chip and the PWB = 8 ppm
- Differential temperature between 25 and 150°C = 125°C
- Distance between the center of the die to the outermost interconnect = 9.5mm

From the calculation, it was found that the amount of free expansion was 9.5μm. Therefore, it was determined that the distance between the center of the chip to the outermost pad at 25°C should be decreased by 9.5μm to compensate for the expansion. Therefore, the new distance between the center of the chip to the outermost pad at 25°C should be 9.4905 mm. Since there are 95 pairs of pads for the outermost row from the centerline of the chip, the distance of each pitch is reduced at 25°C which equates to a new pitch of 99.9μm for each pair of pads. This would allow the distance of each pitch at 150°C to be aligned. Figure 5-4 displays the original layout and revised layout of the PWB side of the assembly.



(a) Original Layout of the PWB at 25°C.



(b) Revised Layout of the PWB at 25°C.

Figure 5-4: Schematic of the (a) Original Layout (b) Revised Layout

5.2. Assembly

Once the dimensions/layout of the daisy chains on the PWB is established, the next steps in the assembly process is to prepare the PWB for assembly of the interconnects. Materials/processes such as soldermask, surface finish of the copper pad, flux selection, and reflow profile of the solder are variables that influence the resultant connection made.

5.2.1. Soldermask

With the PWB at a 100μm pitch it is crucial to have soldermask be deposited over all parts of the board, except where solder joints are to be made. Soldermask is a heat-resisting coating that is applied to prevent deposition of solder on areas that it is not intended. Also, it prevents solder bridging between conductive tracks. Other functions of solder mask are as follows:

- Control of outer layer impedance
- Minimize damage to the board during handling
- Increase corrosion and flammability resistance

With a total stand-off height of 80μm, it is critical to have a very thin layer of soldermask so that it does not prevent the interconnect from not reaching the respective pads on the PWB. Probimer 81 liquid photoimageable soldermask is the soldermask material applied onto the surface of the board and copper pads. The thickness of the soldermask is 3 – 4μm on top of the copper pads. Due to the fine pitch, the board is soldermask defined with a pad openings 35 - 40μm in diameter.

5.2.2. Surface Finish

A combination of nickel and gold and 60Sn/40Pb solder is used as the surface finish, where the nickel is ~2-3μm, the gold is <1μm and the solder is ~15-20 μm. In this study the solder is electroplated onto the surface of the substrate. However, solder can also be stencil printed onto the substrate. Figure 5-5 displays a cross section of the PWB process parameters.

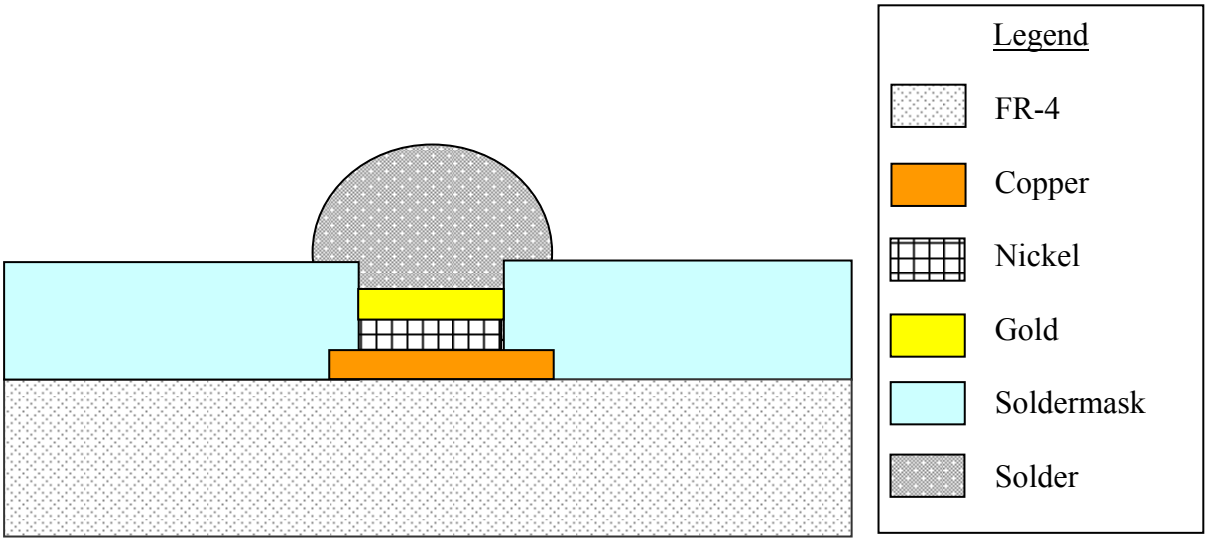


Figure 5-5: Cross Section of FR-4 with surface finish.

5.2.3. Pick and Place

To assemble the die onto the PWB, a semi-automated machine is used to perform the process. RD Automation® M10 flexible flip chip/ die bonder cell is the equipment used to assemble the interconnects. The machine incorporates a self-heating station so thermo-compression bonding can be performed.

Figure 5-6: RD Automation M10 Flexible Flip Chip/ Die Bonder.

Optical alignment is used to obtain good assembly accuracy. The fiducials on the die and PWB are used for aligning the two together. The M10 has an optical camera which can superimpose and image of the fiducials on both the die and PWB to ensure that the alignment is indeed good. Figure 5-7 displays the rough locations and dimensions of the fiducials on the board side that will be used for assembly.

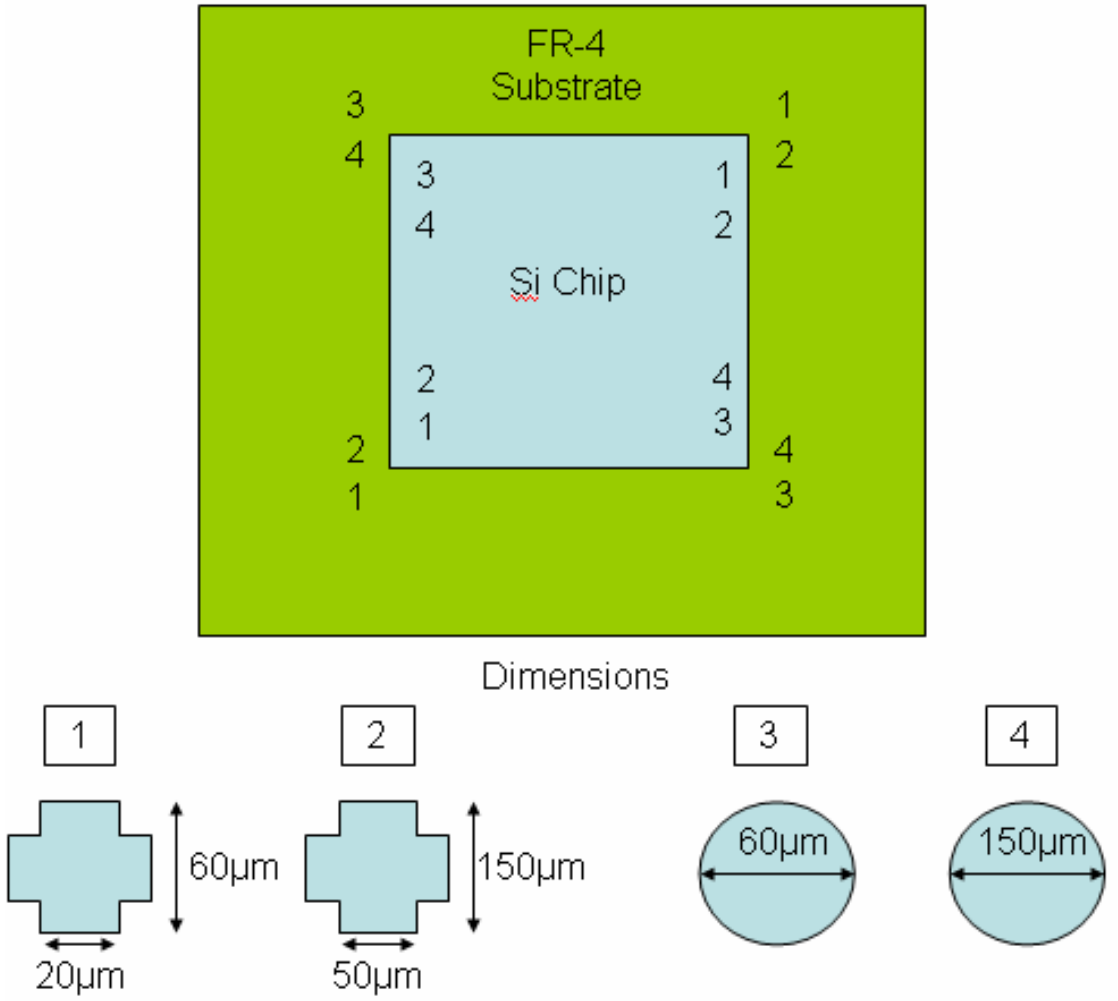


Figure 5-7: Fiducial dimensions and Locations on the PWB.

Once the fiducials are found and noted with the equipment for both the chip and substrate, the equipment can calculate the X, Y, and theta (θ) offsets. Throughout this process the optical microscope can view the fiducials on the chip, substrate, or superimpose the fiducials on both the chip and PWB to ensure that the interconnect is indeed in align with the landing pad. To be able to have optimal alignment, the resolution of the M10 is ±1µm.

Coplanarity

In the assembly of fine-pitch components, one critical concern that the industry needs to overcome is coplanarity of the PWB land areas. Coplanarity is defined as the variation of the land areas on the PWB relative to the other land areas in the array. Figure 5-8 visually depicts the coplanarity issue.

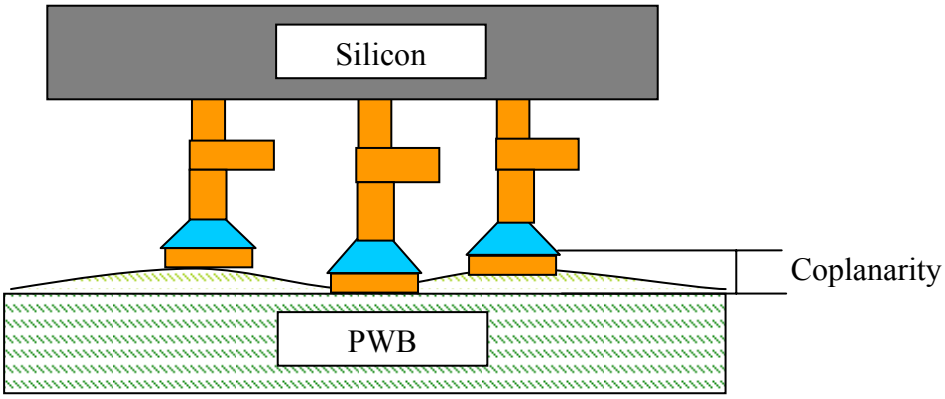


Figure 5-8: Coplanarity Concerns on the PWB.

If conventional solder ball is utilized for fine pitch applications, coplanarity poses an issue because if a bump is considerably smaller than the other balls in the array, it may not form a proper solder joint. This would subsequently result in an open after reflow. With regards to the G-Helix, due to its compliant nature in all directions, it has the inherent ability to compensate for the coplanarity issue. Therefore, during assembly, the G-Helix would compensate for the coplanarity issues where some of the interconnects would compress more than others so that all the interconnects come into contact with the corresponding landing pads on the PWB. To prevent excessive deformation, there are copper columns on the four corners that are 42μm thick. Therefore there is as much as

~30μm of travel for the G-Helix to compensate for the coplanarity of the PWB and interconnects relative to each other.

5.2.4. Flux Selection

Prior to assembly, flux is applied onto the board. Flux is applied to reduce the oxides on the surfaces to be soldered. Depending on the type of solder used, the flux should activate first (I.E. at 150 - 160°C for tin/lead solder) to provide a deoxidized surface until the wetting of the solder. Fluxes are typically classified based on the activity level:

- R (rosin): On-activiated fluxes (no activators)
- RA (rosin-activated): Most active flux and corrosive
- RMA (rosin mildly activated): Mildly activated flux requires good solderability on solder pads and components

For the 60Sn/40Pb solder that is to be assembled, the flux selected was a liquid flux #5 RMA. The RMA is a no-clean flux which does not require any washing after soldering. It should be noted that when applying the flux onto the PWB, to apply a minimal amount. This is because if the layer of flux is too thick, the solder on the board will not be able to wet the interconnects.

5.2.5. Reflowing Solder

Reflowing solder comprises of having the solder that is either electroplated and/or stencil printed onto the PWB, or on the bottom post of the G-Helix heated up to the

melting temperature of solder. This subsequently creates a connection as the interconnects on the silicon side wet the solder on the PWB at the reflow temperature of solder. The process of reflowing the solder should be monitored carefully as the reliability of the solder joint is subject in part to the reflow profile used. The reflow profile can be characterized and broken down into four different phases: pre-heat, thermal soak, reflow, and cool down. Figure 5-9 displays and example of the reflow profile used for 60Sn/40Pb solder.

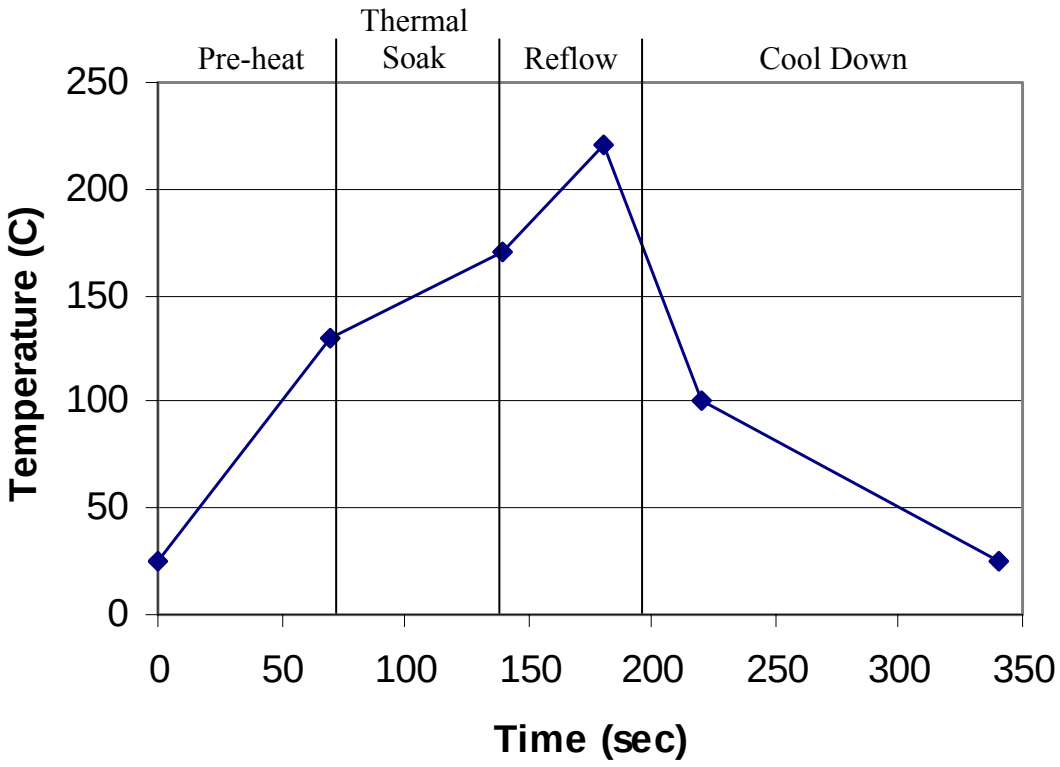


Figure 5-9: Reflow Profile Used for 60Sn/40Pb Solder.

Pre-Heat

The main purpose of the pre-heat stage is to increase the temperature of the die and PWB at a controlled rate to minimize any thermal damage. Therefore, the ramp rate for the pre-heat stage was set at 1.5°C/sec. It should also be noted that if the ramp rate is increased too high, the solvent that is used to regulate the viscosity will not be allowed to evaporate slow enough. As a result, the solvent in the paste may start boiling which causing short circuits between leads. The stage is preheated to 125°C and the die and PWB are not in contact with each other throughout the preheat zone.

Thermal Soak

The thermal soak phase is present to equalize the temperature of all surfaces being soldered. The flux is chemically activated to reduce the metal oxides and expose the clean solderable metal. The interconnect is brought in contact with the PWB with a constant force of 150g. The assembly should stay within this zone anywhere between 60 – 120 seconds. Longer dwell times should be avoided because they may evaporate the flux producing voids in the solder joints.

Reflow

In the reflow zone, the 60Sn/40Pb solder reaches its liquidus stage at ~183°C. The assembly is rapidly heated at temperatures above 183°C so that the solder wets the copper pads on the PWB and intermetallic layers form. The peak temperature of the assembly is normally around 210 - 220°C to ensure adequate fluxing and solder flow to obtain good wetting. However, if this temperature is too high and is held for a long duration, it may damage the components and create excessive intermetallic layers.

Therefore, it would have a negative impact on the reliability of the interconnection. Thirty to ninety seconds at temperatures above 183°C is sufficient to form a good electrical and mechanical connection. In this zone of the reflow profile, a constant 150 gram load is applied onto the interconnects to hold the interconnects in place and ensure proper adhesion.

Cool Down

Once the connection is made, the cool down phase is the last zone the assembly goes through. This allows the solder to solidify before being unloaded from the assembly tool. It is very important to control the cooling rate of the assembly because it determines the grain size of the solder. Faster cooling rates produce a smaller grain size. However, if the cooling rate is too fast, it may result in damage to the assembly due to the different CTE expansion and contraction rates. If the solder is not cooled fast enough, larger grains will form which provide a weak connection. Therefore, the cooling rate is set to be between 2°C/sec - 4°C/sec. A constant load of 150g is applied until the assembly is cooled to 150°C, then the chuck vacuum is turned off.

5.2.6. Best Known Methods for Assembling Compliant Interconnects

Due to the nature of free-standing complaint interconnects, assembly of G-Helix is not a trivial task. Prior to assembly of the G-Helix interconnects onto an organic substrate, the interconnects are assembled onto a glass substrate which has 15μm high and 40μm diameter solder balls electroplated onto the surface. Assembling onto glass substrates provides a quick and easy way to inspect the assembly and to develop a "Best Known Methods (BKM)" methodology for assembling compliant interconnects.

In the assembly of the interconnects, some of the critical parameters which can be manipulated are as follows:

- Volume of flux
- Temperature profile
- Force profile during assembly
- Reflow time

Depending on value of the various parameters, they can change the resultant assembly. Since the M10 flip-chip bonder has the capability of applying a thermo-compression bonding. The temperature and force at which they are applied is critical to the resultant bond that is created. For instance, if too much force is applied (> 450g), the excessive force would deform the G-Helix such that the arcuate beam would wick onto the neighboring solderball. Figure 5-10 and Figure 5-11 provides an example of what occurs when excessive force is applied.

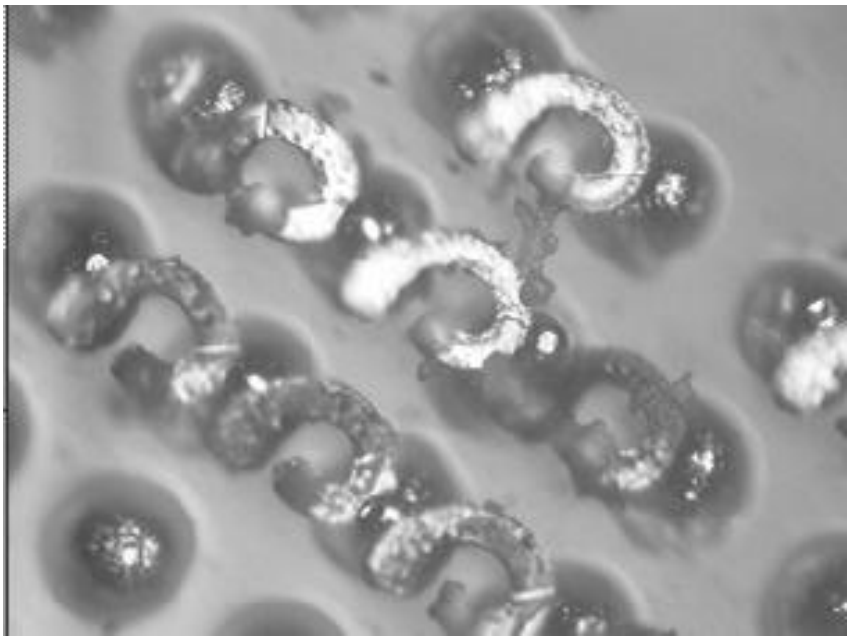


Figure 5-10: Interconnect Misalignment and Solder Wicking From Neighboring Solderball.

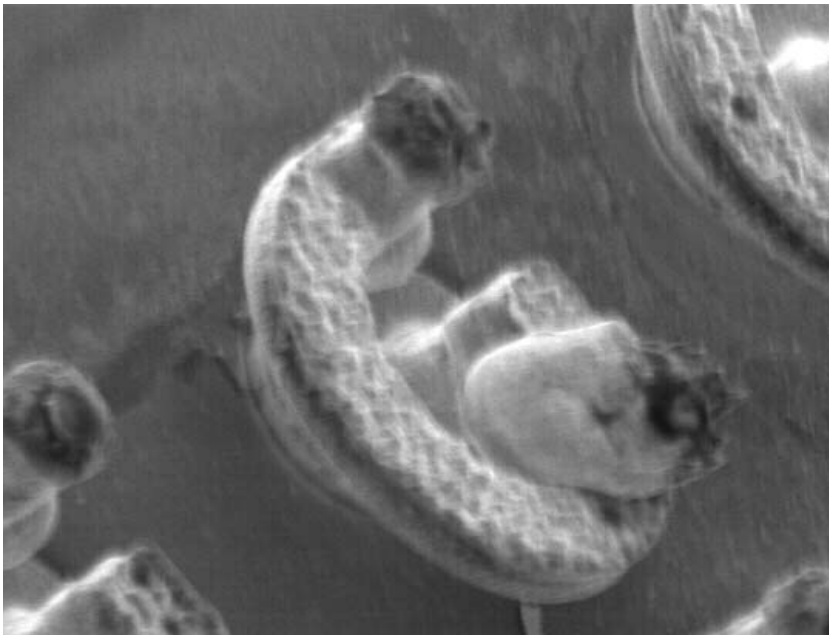


Figure 5-11: Solder wicking onto the arcuate beam.

Another issue which cause poor bonding and misalignment was because of the volume of flux that was applied. Therefore, when applying the flux, a minimal amount of flux should be applied onto the substrate so that the top post of the G-Helix maybe able to

penetrate the flux and subsequently obtain a good bond. Once the various parameters were optimized by determining the optimal force, thermal profile, and flux volume, assembly of the G-Helix was shown to be successful on a glass substrate. Figure 5-12 displays an example of a successful assembly onto a glass substrate.

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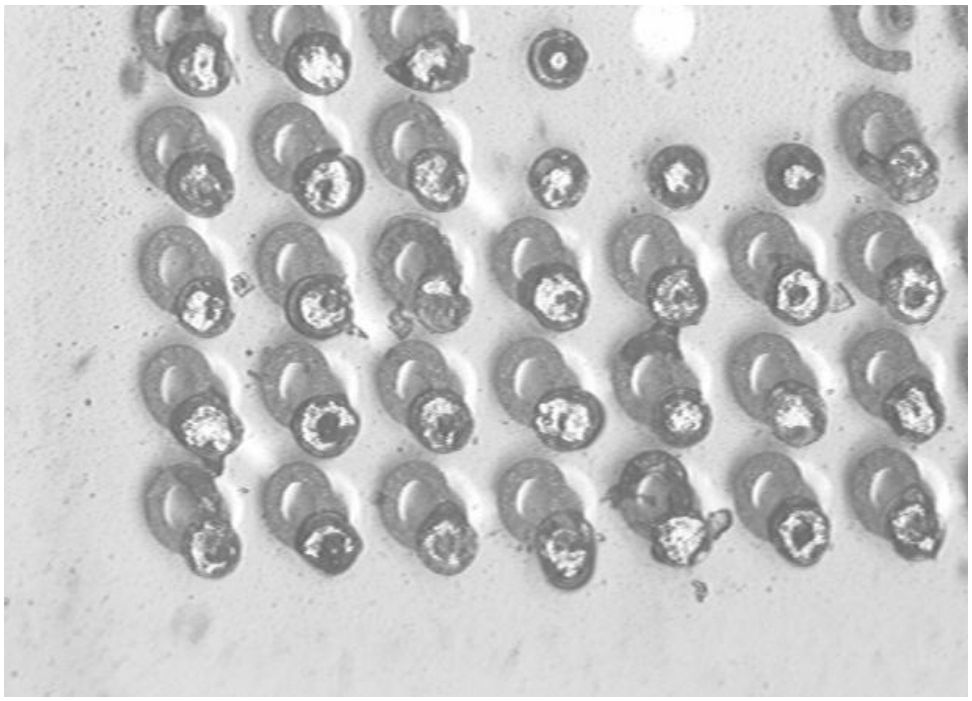


Figure 5-12: View of Back Side of Assembly Onto a Glass Substrate.

It should be noted that when a small force (~150g) is applied on the substrate, that it does not excessively deform the interconnects. Therefore, after inspecting through the backside of the glass substrate, no solder wicked onto the arcuate beam of the G-Helix.

5.2.7. Assembly onto Organic Substrate

Incorporating the reflow and assembly load profile discussed in 5.2.5, assembly was performed on organic substrates. To ensure that the alignment of the assembly is good, on an organic substrate X-ray can be used. X-ray inspection equipment produce

gray-scale images that represent variances in the shape and thickness of an object. Thick and high-density features will produce a darker image than those with lesser density or thickness. Therefore, a correlation between acceptable or unacceptable features and manufacturing processing conditions can be quantitatively measured. Figure 5-13 displays the methodology of the X-ray Equipment.

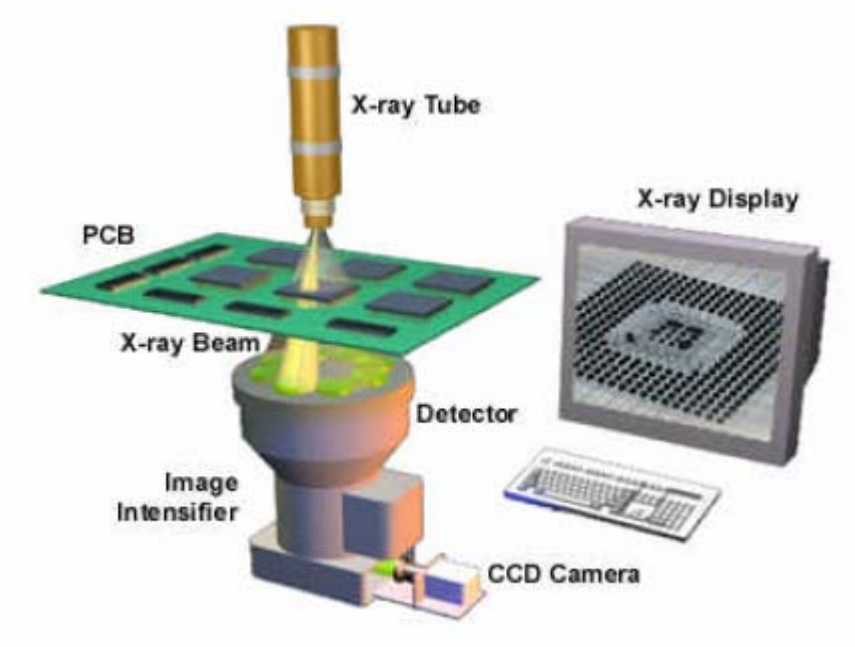


Figure 5-13: X-ray methodology [Teradyne 2004].

X-ray inspection can reveal a number of issues such as how well the alignment is between the G-Helix and the corresponding landing pads on the PWB. It can also detect defects, whether hidden or visible, including open or shorted solder joints, lifted leads, voiding, and unacceptable size variations in the G-Helix and solder bumps. With regards to the G-Helix assembly, the X-ray equipment was used and Figure 5-14 provides an example of the assembly.

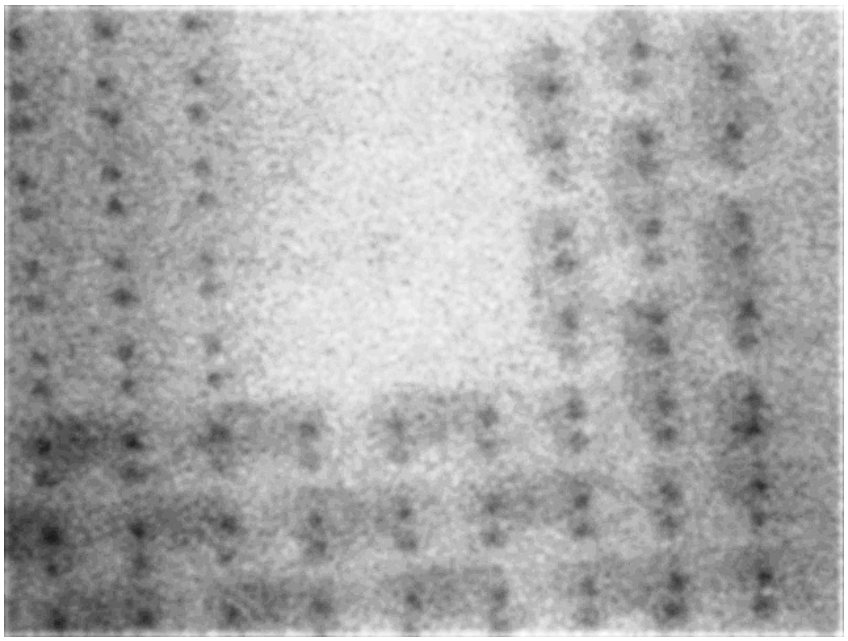


Figure 5-14: X-ray image of the G-Helix assembly.

As can be seen from the image, the alignment of the assembly is good. However after probing the daisy chains around the die for continuity, two chains were obtained. Figure 5-15 provides the location of where continuity was obtained for the G-Helix.

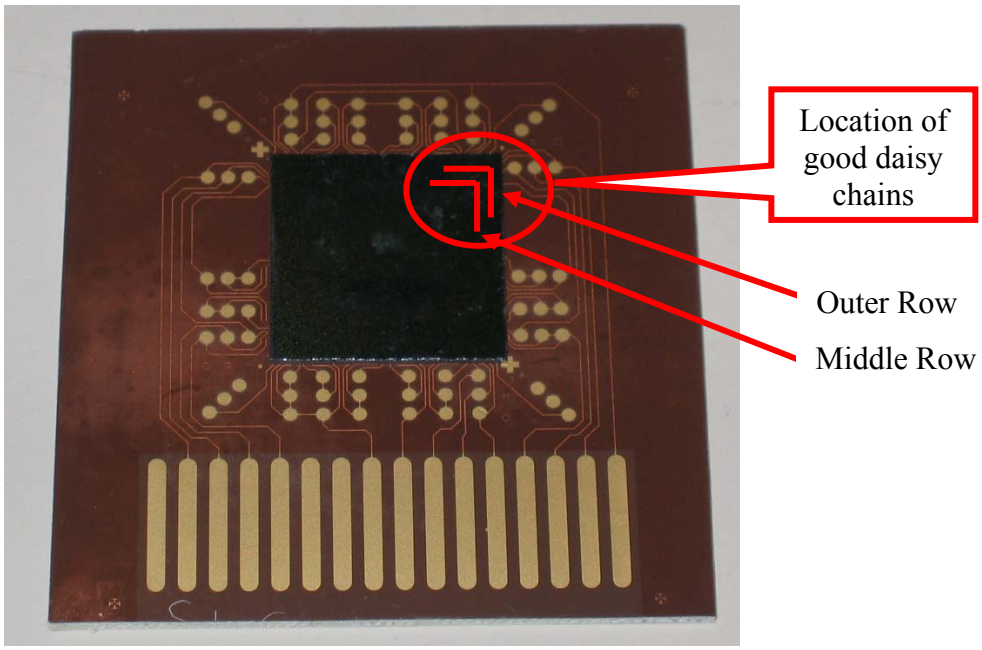


Figure 5-15: Assembled G-Helix Interconnects onto an Organic Substrate.

5.3. Reliability Assessment of G-Helix

Reliability is defined as the probability that a component or assembly will be operational for the expected period of use [Tummala 2001]. When microelectronic packages are subjected to actual field use, failures in the product are typically seen at the system level. However, the cause of the failure are always observed at the component level which is due to thermal, mechanical, electrical, or a combination of these failure modes and mechanisms. To assess the reliability and qualify a product within a reasonable amount of time in a well-controlled environment, accelerated tests can be performed. In these accelerated tests, they are performed to obtain reliability data in a much shorter period of time, and an acceleration factor is used to convert the time-to-failure under accelerated test conditions to the actual time-to-failure under normal usage conditions [Tummala 2001]. In this section, the experimental details of accelerated thermal cycling of the compliant interconnects will be will be discussed.

5.3.1. Experimental Setup and Results

A commonly accepted thermal cycling profile for microelectronics is by JEDEC (JESD22-A104-B), test condition J and thermal soak 4, which thermal cycles the package between 0°C and 100°C with fifteen minute dwells [JEDEC 2000]. The ESPEC air-to-air thermal chamber at Georgia Tech is used to thermal cycle the assembly.

Figure 5-16: ESPEC Thermal Chamber.

The ESPC has two chambers to perform the thermal cycle testing where the top chamber is at 100ºC and the lower is at 0ºC. The system has a basket for samples to be placed onto. Thermal cycling is performed between 0 ºC to 100 ºC. The sample is run continuously for 100 cycles. After the end of the 100 cycles, the samples are removed from the chamber to be inspected. The electrical resistance of the daisy chain is measured at room temperature. An open chain is based off of IPC guidelines for accelerated reliability testing (IPC-ZSM-785) which states that "electrical discontinuity is indicated by a loop resistance of 1000 ohms or more" [IPC 1992].

The corresponding chains on the assembly that were monitored is shown in Figure 5-15 where the daisy chain located on the outermost row will be designated as "Outer Row", and the middle row is "Middle Row". Prior to placing the sample into the thermal chamber the resistance of the two chains is measured. The resistance measurement and subsequent measurements at various increments will be noted until failure of the daisy chain.

Table 5-1: Resistance Measurements of the Daisy Chain.

	Resistance Measurement at Corresponding Number of Thermal Cycles (Ω)			
Location	**0**	**100**	**275**	**440**
Middle Row	11.6	11.7	11.8	12.0
Outer Row	8.6	8.7	8.7	8.8

The two daisy chains have currently passed 440 accelerated thermal cycles. The reliability assessment is still currently ongoing.

CHAPTER 6

MATERIAL MODELING

In parallel to experiments that are performed, numerical models will be discussed. The G-Helix assembly consist of silicon, organic substrate, copper which defines the G-Helix and solder used to attach the compliant interconnect onto the organic substrate. The following chapter presents the material constitutive modeling for the various components which constitute the G-Helix assembly. Direction-, temperature, time-dependent, and time independent material constitutive properties will be incorporated as appropriate.

6.1. Silicon Die

Silicon is the most widely used semiconductor material in microelectronics because of its material properties and it can be extracted from silica relatively easy. Electronic devices such as PN junction diodes can be engineered and designed on top of the silicon material. The silicon die is modeled as isotropic, linear-elastic, and temperature dependent. Table 6-1 provides the CTE, Poisson's ratio, and Young's modulus for silicon die that were used in this study.

Table 6-1: Material Properties for Silicon Die [Zhu, 1999]

Material Property	Value
CTE (α)	2.6 ppm/^{o}C
Poisson's Ratio (v)	0.25
Young's Modulus (E) at 0°C	120.85 GPa
Young's Modulus (E) at 50°C	114.85 GPa
Young's Modulus (E) at 100°C	109.85 GPa

6.2. FR-4 Substrate

FR-4 is a flame-retardant composite material, where the FR stands for flame retardancy as designated by the National Electrical Manufacturers Association (NEMA). FR-4 is constructed on multiple plies of epoxy-resin impregnated onto a woven glass cloth. Since the substrate is made up of layers of glass and epoxy, the behavior of the material is orthotropic. The FR-4 used in this research is Hitachi Chemical's high elastic modulus and low CTE material. The material is modeled as linear elastic, temperature dependent and orthotropic. Table 6-2 displays the material properties of FR-4 used.

Table 6-2: Material Properties for FR4 Substrate [Hegde 2003]

T, °C	30	95	110	125	150	270
E_x (MPa)	29400	28100	27800	27500	27000	24600
E_z (MPa)	29400	28100	27800	27500	27000	24600
E_y (MPa)	2000	2000	1880	1700	1400	880
ν_{xz}	0.136	0.136	0.136	0.136	0.136	0.136
ν_{xy}	0.1425	0.1425	0.1425	0.1425	0.1425	0.1425
ν_{yz}	0.1425	0.1425	0.1425	0.1425	0.1425	0.1425
α_x (10^{-6}/°C)	11	11	11	11	11	11
α_z (10^{-6}/°C)	11	11	11	11	11	11
α_y (10^{-6}/°C)	27	30	32	35	40	114

6.3. Electroplated Copper

To fabricate the G-Helix, it comprises of electroplated copper. The copper is modeled as isotropic, temperature dependent, multi-linear kinematic hardening relationship. Kinematic hardening represents a uniform translation of the yield surface which can represent the Bauschinger effect and it was shown in previous publications that copper exhibits this type of behavior [Lubliner 1990]. Table 6-3 and Table 6-4 display the material properties for copper.

Table 6-3: Material Properties for Copper [Iannuzzelli 1991].

Temperature (°C)	E (GPa)	ν	α (10^{-6}/°C)
27	121.0	0.3	17.3
38	119.0	0.3	17.3
93	117.0	0.3	17.3
149	115.0	0.3	17.3
204	112.0	0.3	17.3
260	110.0	0.3	17.3

Table 6-4: Stress-Strain Relationship for Copper [Iannuzzelli 1991].

Strain	σ (MPa) At 27°C	σ (MPa) At 260°C
0.001	121	110
0.004	186	179
0.01	217	214
0.02	234	231
0.04	248	245

6.4. Solder

To ultimately assemble the G-Helix onto the substrate, solder is used. In general, if the absolute temperature of solder is greater than half the absolute melting temperature of the material, the material will exhibit creep behavior. Therefore, the inelastic deformation of the material should take into consideration time-dependent plasticity (creep) along with time-independent plasticity. Therefore, the material modeling of solder should include inelastic strains that constitute rate-independent plasticity along with rate-dependent deformation behavior either in an explicit creep equation or combine the inelastic strains into a unified viscoplastic model [Anand, 1985, McDowell 1994]. The following section discusses material modeling to represent the behavior of 63Sn/37Pb, 95.5Sn/3.8Ag/0.7Cu, 60Sn/40Pb, and 96.5Sn/3.5Ag solders.

6.4.1. Elastic-Plastic/Creep 63Sn/37Pb Solder

63Sn/37Pb solder also known as "eutectic' tin-lead solder is modeled with as isotropic, temperature dependent, multi-linear kinematic hardening with power law creep [CINDAS 1995, Ju 1994]. Table 6-5 and Table 6-6 provide the temperature dependent material properties for 63Sn/37Pb at strain rate of 0.0081/sec. The elastic modulus is the value of the modulus is the slope of the first segment of the stress-strain curve. The shear modulus for 63Sn/37Pb solder was determined according to Equation 6-1.

$$G = \frac{E}{2*(1+2\nu)} \qquad 6\text{-}1$$

Table 6-5: Stress-Strain Relationship for 63Sn/37Pb [CINDAS 1995].

Strain	σ (MPa) At -25°C	σ (MPa) At 25°C	σ (MPa) At 85°C	σ (MPa) At 125°C
0.001	27.39	19.65	15.27	11.68
0.002	41.36	29.68	22.51	16.12
0.003	47.93	34.12	26.00	18.56
0.004	50.30	36.35	27.83	19.88
0.005	50.77	37.24	28.64	20.55

Table 6-6: Temperature Dependent Properties for 63Sn/37Pb [CINDAS 1995].

T, °C	-25	25	85	125
$E_x = E_y = E_z$ (Mpa)	27390	19650	15270	11680
$\nu_{xz} = \nu_{xy} = \nu_{yz}$	0.4	0.4	0.4	0.4
$G_{xz} = G_{xy} = G_{yz}$ (MPa)	9782	7018	5454	4171
$\alpha_x = \alpha_y = \alpha_z$ (10^{-6}/°C)	21	21	21	21

With regards to the time-dependent characteristic of 63Sn/37Pb solder, the steady state it is modeled using a power-law (Norton creep law) which takes the form of Equation 6-1.

$$\dot{\varepsilon}_c = A\sigma^n e^{-(Q/R_g T)} \qquad 6\text{-}1$$

The constants for Equation 6-1 are shown in Table 6-7.

Table 6-7: Creep Constants for 63Sn/37Pb [Ju 1994].

Constant	Value
A	$1.84 \times 10^{-4} \ \frac{1}{MPa * s}$
n	5.2
Q	50 kJ/mol
R_g	8.314×10^{-3} kJ/mol-K

6.4.2. Elastic-Plastic/Creep 95.5Sn/4Ag/0.5Cu Solder

One type of lead-free solder investigated is 95.5Sn/4Ag/0.5Cu. It is modeled with isotropic, temperature dependent, multi-linear kinematic hardening with Norton creep law [Wiese 2002]. Table 6-8 and Table 6-9 provide the temperature dependent material properties for as cast 95.5Sn/4Ag/0.5Cu at four temperatures. It should be noted that the material parameters obtained from Wiese's paper were only provided at 0°C and 50°C. Therefore, the data for the -55°C and 100°C were extrapolated data.

Table 6-8: Stress-Strain Relationship for 95.5Sn/4Ag/0.5Cu [Wiese 2002].

Strain	σ (MPa) At -55°C	σ (MPa) At 0°C	σ (MPa) At 50°C	σ (MPa) At 100°C
0.0014	62	57.4	53.2	35
0.004	90.667	80	72	45.6
1	3300	2500	1900	1318

Table 6-9: Temperature Dependent Properties for 95.5Sn/4Ag/0.5Cu [Wiese 2002].

T, °C	-55	0	50	100
$E_x = E_y = E_z$ (Mpa)	44300	41000	38000	25000
$\nu_{xz} = \nu_{xy} = \nu_{yz}$	0.36173	0.36173	0.36173	0.36173
$\alpha_x = \alpha_y = \alpha_z$ (10^{-6}/°C)	22	22	22	22

With regards to the time-dependent characteristic of 95.5Sn/4Ag/0.5Cu solder, the steady state it is modeled using a Norton creep law which takes the form of Equation 6-1. The constants for Equation 6-1 are shown in Table 6-10

Table 6-10: Creep Constants for 95.5Sn/4Ag/0.5Cu [Wiese 2002].

Constant	Value
A	1.84 x 10-4 $\frac{1}{MPa * s}$
n	1
Q	83.1 kJ/mol
R_g	8.314x10-3 kJ/mol-K

6.4.3. Viscoplastic Model for 60Sn/40Pb Solder

To model the plastic deformation for 60Sn/40Pb, Anand's viscoplastic model which combines the rate dependent and rate independent deformation mechanisms is used. To incorporate Anand's model, the elastic modulus, poisson's ratio, and CTE also need to be defined. Equation 6-2 is used to obtain the shear modulus at a temperature T and using Equation 6-1, the temperature-dependent Young's modulus can be obtained [Lau 1997].

$$G(tT) = G_0 - G_1 T \qquad 6\text{-}2$$

The constants used for Equation 6-2 are displayed in Table 6-11 for 60Sn/40Pb.

Table 6-11: Elastic shear constants, CTE, and Poisson ratio for 60Sn/40Pb solder [Lau 1997].

	Value
G_o (MPa)	$1.3x10^4$
G_1 (MPa)	56
α (10^{-6}/°C)	$24.5x10^{-6}$
ν	0.4

Table 6-12 displays the constants for Anand's model for 60Sn/40Pb [Wang 2001].

Table 6-12: Constants for Anand Model for 60Sn/40Pb solder [Wang 2001].

Meaning	Wilde's Constants for Anand's Model
s_o (MPa)	56.33
Q/R (K)	10830
A $(\sec^{-1})$	1.49×10^7
ξ	11
m	0.303
h_o (MPa)	2640.75
$\hat{s}$ (MPa)	80.42
n	0.0231
a	1.34

6.4.4. Viscoplastic Model for 96.5Sn/3.5Ag Solder

To model the plastic deformation for 96.5Sn/3.5Ag, Anand's viscoplastic model is used. To incorporate Anand's model, the elastic modulus, poisson's ratio, and CTE also need to be defined. Equation 6-2 is again used to obtain the shear modulus at a temperature T and using Equation 6-1, the temperature-dependent Young's modulus can be obtained [Lau 1997].

The constants used for Equation 6-2 are displayed in Table 6-13 for 96.5Sn/3.5Ag.

Table 6-13: Elastic Shear Constants, CTE, and Poisson ratio for 96.5Sn/3.5Ag solder [Lau 1997].

	Value
G_o (MPa)	1.931×10^4
G_1 (MPa)	68.9
α (10^{-6}/°C)	24×10^{-6}
ν	0.4

Table 6-14 displays the constants for Anand's model for 96.5Sn/3.5Ag [Wang 2001].

Table 6-14: Constants for Anand Model for 96.5Sn/3.5Ag solder [Wang 2001].

Meaning	Wilde's Constants for Anand's Model
s_o (MPa)	39.09
Q/R (K)	8900
A $(\sec^{-1})$	2.23×10^4
ξ	6
m	0.182
h_o (MPa)	3321.15
$\hat{s}$ (MPa)	73.81
n	0.018
a	1.82

CHAPTER 7

VIRTUAL RELIABILITY ASSESSMENT OF G-HELIX PACKAGE

In this chapter the thermo-mechanical reliability of G-Helix interconnects is assessed through numerical models. As the helix assembly comprises of 2256 interconnections, and due to the 3D nature, nonlinear material properties, and complexity of the geometry, the system of equations in the finite element model can be very large and takes a good amount of computational time to obtain a solution. Therefore, approximations were made to represent the actual geometry of the package. Generalized Plane Deformation (GPD) and quarter symmetry models incorporating equivalent beams were developed to simplify the model without sacrificing much on the accuracy of the model.

7.1. G-Helix Package Construction

The G-Helix assembly comprises of a silicon die, G-Helix interconnects, solder paste, copper pads, and FR-4 substrate. Figure 7-1 displays the schematic of the G-Helix package assembly analyzed.

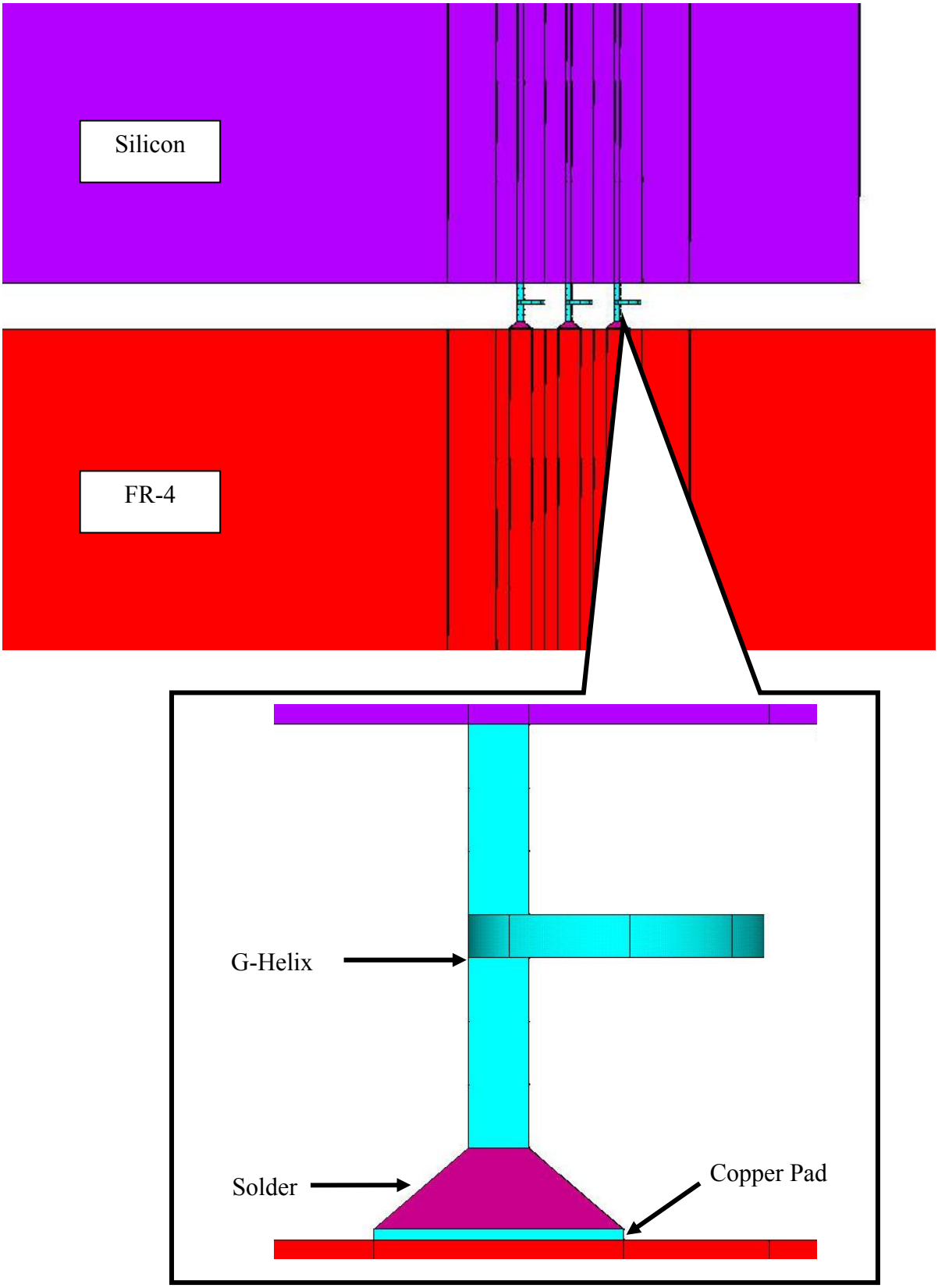


Figure 7-1: Schematic of the G-Helix Assembly.

The planar dimension of the silicon die is 20 x 20mm with a thickness of 0.5mm. Also, the package is assumed to be chip scale, therefore the length of the FR-4 is 10% larger than the silicon die, which is 22 x 22mm with a thickness of 1.25mm. The dimensions of the G-Helix were obtained from the optimization performed from previous work and is provided in Chapter 2. As for the solder paste, it is assumed to have a height of 15μm with a base width and thickness equivalent of that for the copper pad on the PWB which is 40 x 40μm. The copper pad is 3μm thick. The interconnect pitch is 100μm and is a three-row peripheral array comprising of a total of 2256 G-Helix interconnects. For the present work, the copper pads on the PWB side did not comprise of soldermask, and there is no passive layer on the die side.

7.2. Geometric Modeling for the G-Helix Package

There are a variety of ways that have been developed to characterize the deformation of a microelectronic package. A 2D model utilizing either plane strain or stress boundary conditions cannot be used because it does not accurately capture the deformation of the three-dimensional G-Helix structure. Therefore, the strain distribution cannot be accurately predicted the fatigue life of the structure. However, a GPD or quarter model package can be used to model the 3D stress/strain effects of the G-Helix package.

7.2.1. 3D Generalized Plane Deformation (GPD) Model

A compromise between an accurate 3D model and a computationally efficient 2D model is a GPD (strip model) model [Tunga 2004]. The geometry is represented by 3D elements that represent only a part of the width of the entire package. The GPD model

takes a vertical slice out of the assembly. The width of the model is 100µm, which is the pitch of the interconnects. The section taken out for the GPD model is shown in Figure 7-2.

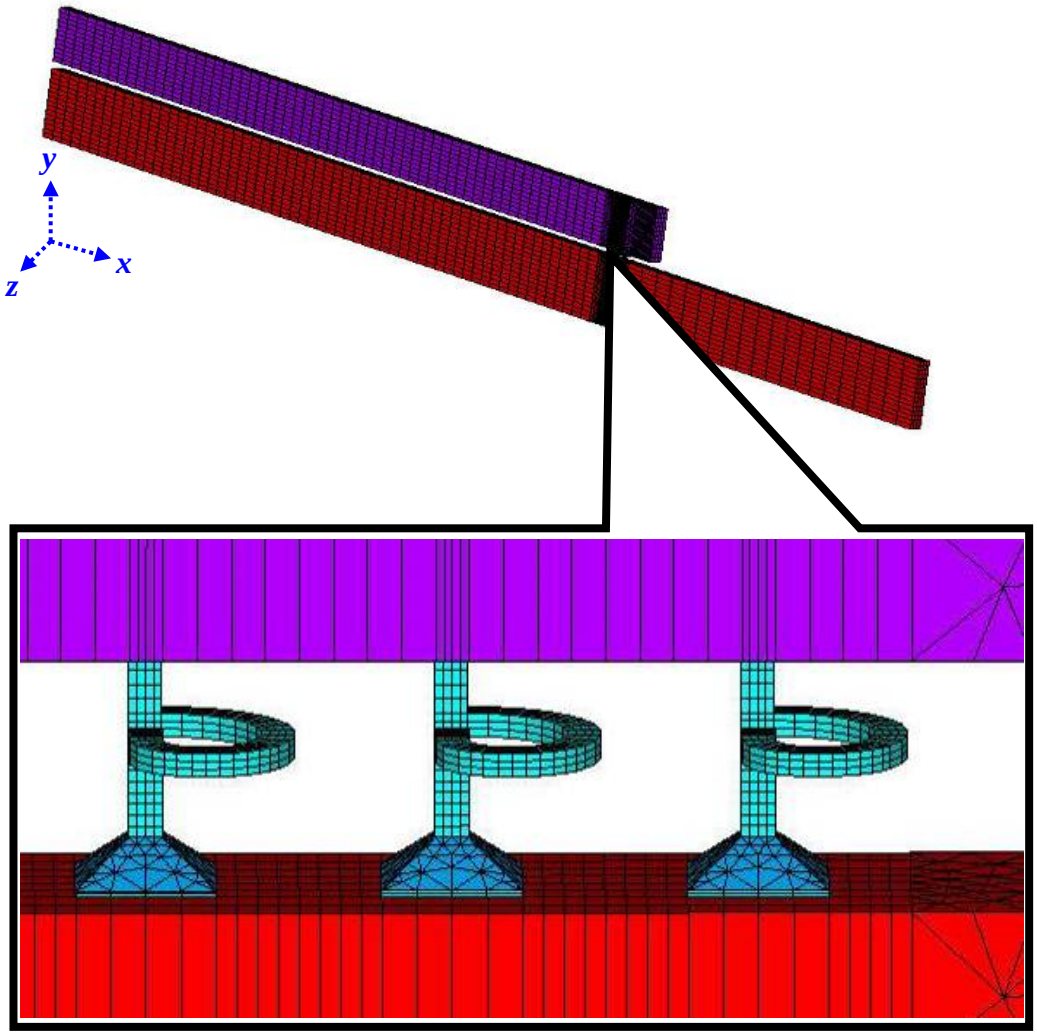


Figure 7-2: GPD Model for the G-Helix Package Assembly.

Due to the symmetry of the package, only half of the package was included in the model. Therefore, the nodes along the axis of symmetry were constrained in the *x*-direction. Also, a single node on the bottom left corner was also constrained in all three directions to prevent rigid body motion. This is shown in Figure 7-3a. In addition, the

two *z*-faces of the strip are coupled so that they displace together in the same magnitude and direction as shown in Figure 7-3b.

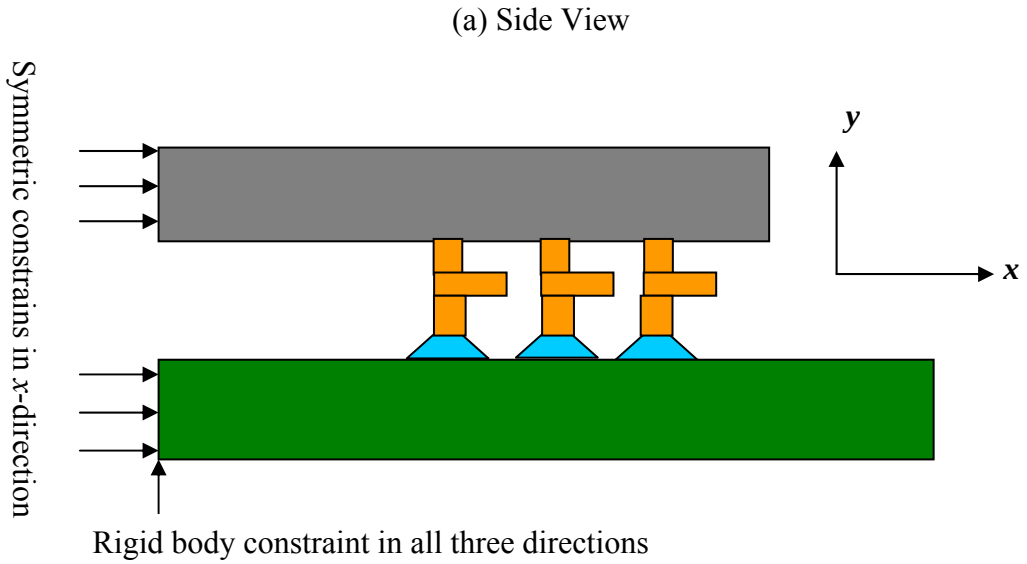


Figure 7-3: Symmetric and Coupling Boundary Conditions of GPD Models

7.2.2. 3D One Quarter Model with Equivalent Beams

To characterize the behavior of the G-Helix microelectronic package, a full 3D model should be incorporated. However, the model can be very difficult to implement and modify for parametric analysis and the computational time can be very high. However, a quarter 3D symmetry model can be used which improves on the GPD model because in a GPD model it only represents a 'slice' of the entire package. Therefore, the GPD model assumes that there is only an array of three interconnects neglecting the fact that in a peripheral array package an array of interconnects on the other edge of the die exist. In a quarter model package, it can capture the deformation effects of the array of interconnects on the two edges of the die. Consequently, a quarter model using equivalent beams is investigated. Figure 7-4 displays the 3D model which possess $1/4^{th}$ symmetry.

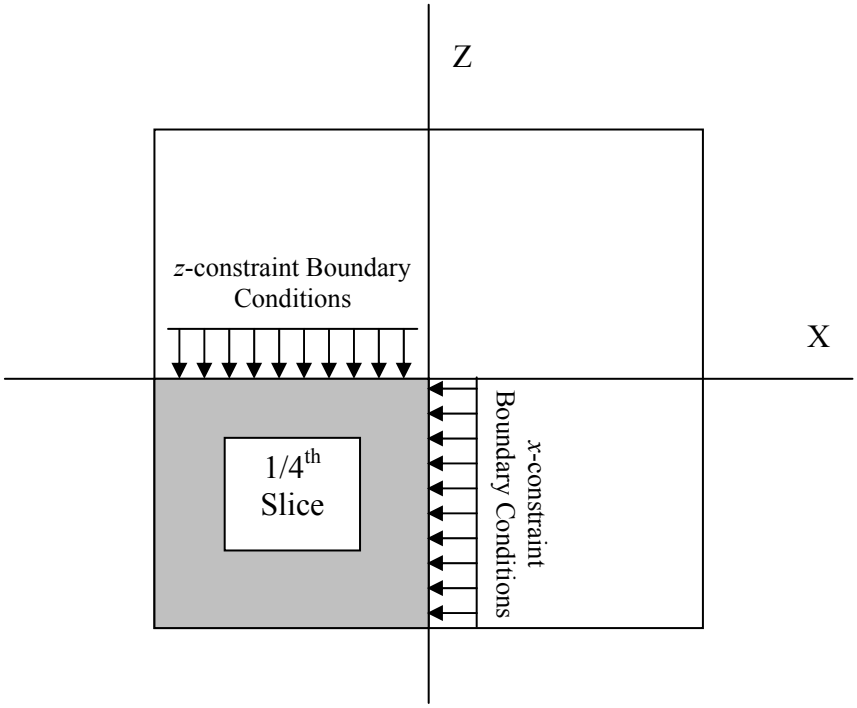


Figure 7-4: Quarter-symmetry model.

As for the global boundary conditions for a quarter symmetry model G-Helix all the nodes on the right most edge are constrained from *x*-displacements and *z*-rotations. As for the top most edge, they are constrained from *z*-displacements and *x*-rotations. Also, a single node on the bottom right corner of the PWB is constrained in all three directions to prevent rigid body motion.

7.3. Equivalent Beam Model

Quarter symmetry model with 500+ interconnects will be computationally time consuming. The number of nodes will also exceed the maximum number of nodes possible in the current version of ANSYS® software. Therefore, equivalent beam elements are used to represent the G-Helix interconnects that are not of interest in the package. However, the corner interconnect which has the furthest DNP is represented by solid elements as this interconnect will be used for fatigue analysis. As for the other interconnects included in the model, they would be represented by equivalent beams such that the deformation characteristics are similar to that of an actual interconnect when subjected to a thermo-mechanical load. The equivalent beam approach minimizes the number of nodes/elements used in the simulation. In the subsequent sections, the methodology used to incorporate equivalent beams into the quarter-model package will be discussed.

7.3.1. G-Helix Characterization

The first step in developing the characteristics of the equivalent beam is to understand the deformation characteristic of the actual G-Helix interconnect. In this section, the G-Helix is modeled and characterized with solder, and a copper pad. It is

assumed that 8μm of the copper post was embedded into the solder for the study. Figure 7-5 displays the meshed compliant interconnect with solder and a copper pad.

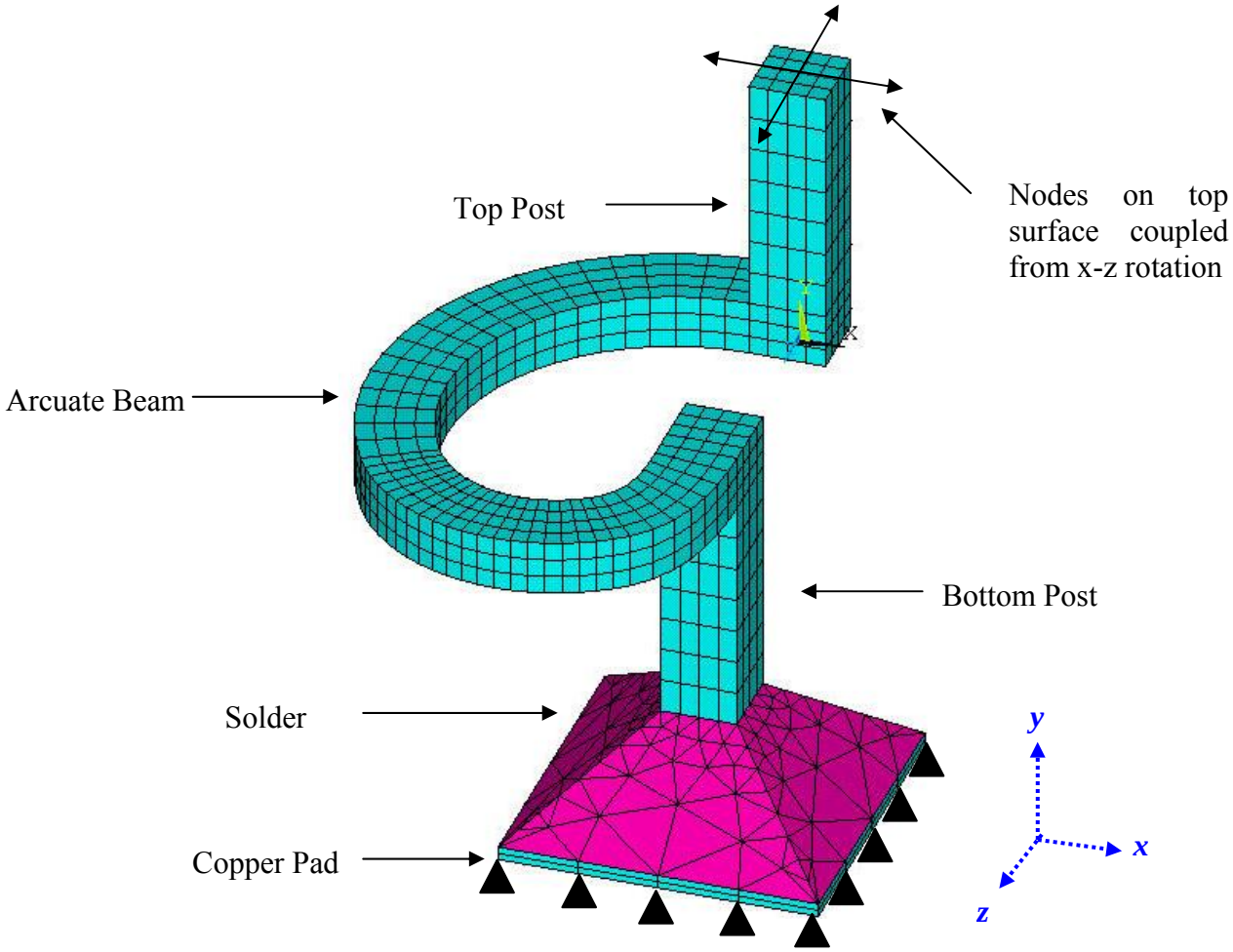
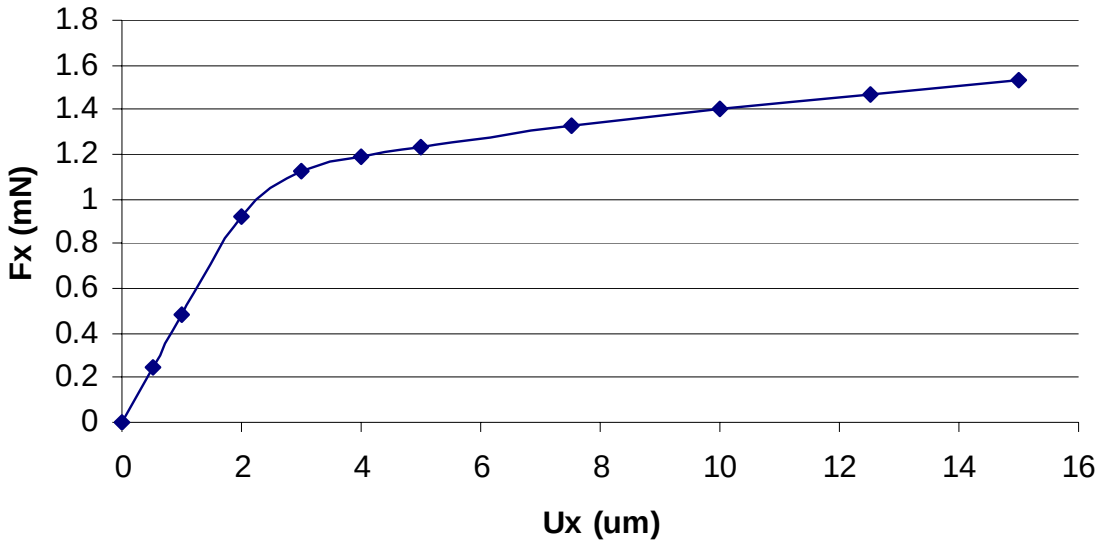


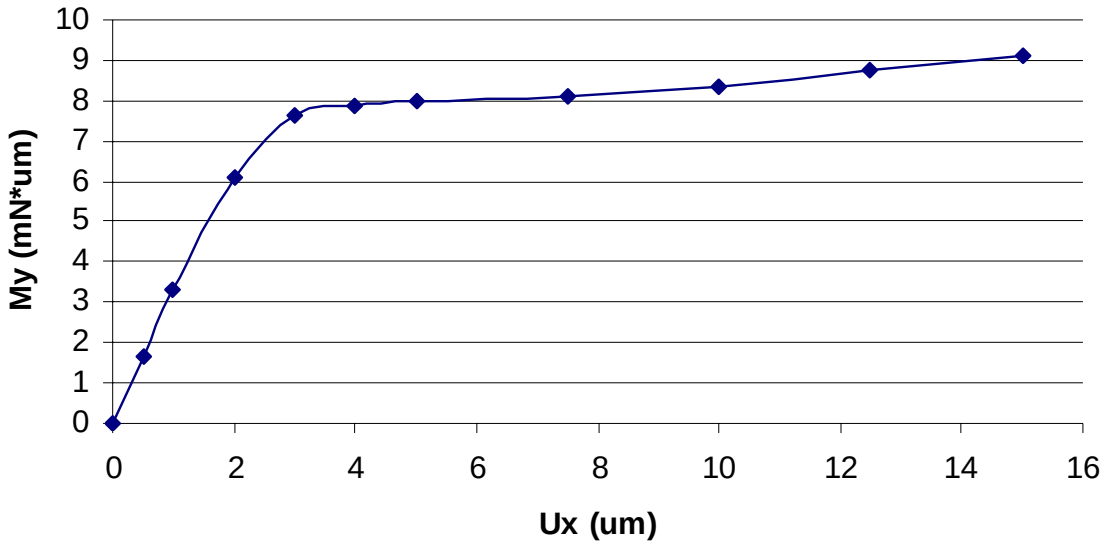
Figure 7-5: G-Helix with Solder.

The boundary constraints on the assembly shown in Figure 7-5 are that the copper pad is constrained from all degrees of freedom, and the nodes on the top post are coupled from in-plane (*x*-*z*) rotation. The coupling of the nodes in the *x*-*z* plane is done to simulate the interconnect in an actual assembly. Therefore in an assembly, the surface of the top post would be perpendicular to the surface of the silicon substrate. This would subsequently prohibit free rotation of the G-Helix. A displacement was applied in the

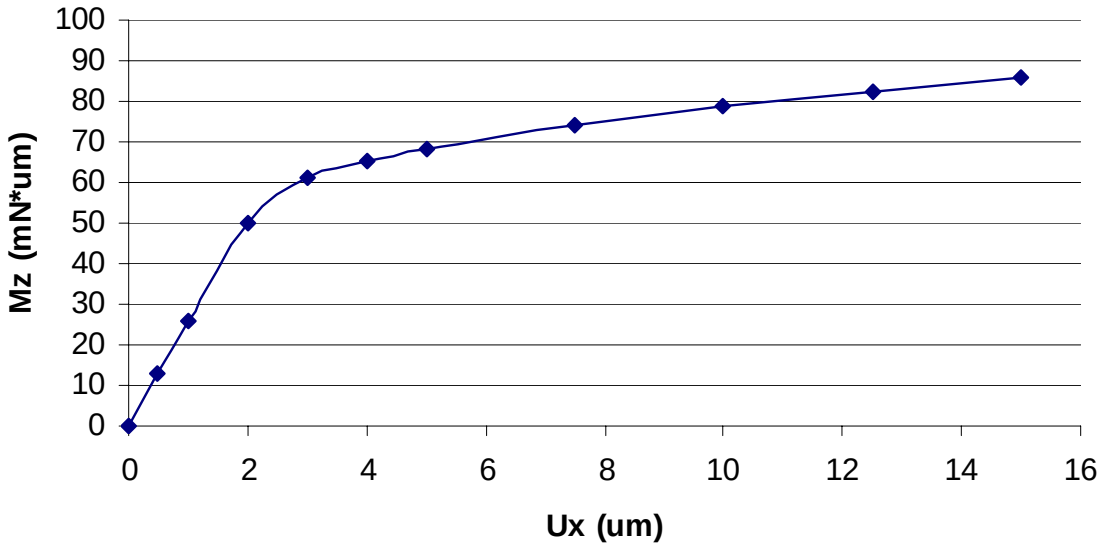
three orthogonal directions in increments between 0.5μm - 15μm in the *x*- and *z*-direction and 0.5μm - 20μm in the y direction. The values of the displacements were assumed to be within the ranges that an actual assembly would be subjected to. Other metrics that are obtained from the actual optimized G-Helix structure are the moments in the other two orthogonal directions relative to the orthogonal direction of displacement. Figure 7-6 displays plots of the force in the *x*-direction and moments in the *y*- and *z*-direction when a displacement was applied in the *x*-direction.



(a) Force in the *x*-direction vs. Displacement in the x-direction



(b) Moment in the *y*-direction vs. Displacement in the *x*-direction.



(c) Moment in the *z*-direction vs. Displacement in the *x*-direction

Figure 7-6: Numerical Simulation of the G-Helix Performance When Displaced in the *x*-direction.

When a displacement is applied the one orthogonal direction (e.g. x), the forces in the other two orthogonal directions (F_y and F_z), and moment (M_x) in the direction of the displacement are not plotted. This is because the magnitude of these forces and moment are close to zero.

7.3.2. Equivalent Beam Characterization

To model a single G-Helix interconnect requires over 1500 elements. Therefore, to incorporate actual interconnects throughout the entire quarter model would exceed the node allotment of the software as well as increase the computational time. In the modeling of a quarter model package, the main objective of the model is to understand the thermo-mechanical reliability of the G-Helix which is the furthest from the neutral point of the die, which corresponds to the interconnect on the outermost corner of the die. Hence, the purpose of the other interconnects in the model are to transfer their characteristic force and moments such that the outermost interconnect would see the type of deformation when subjected to a thermal loading. As a result, the equivalent beam can be used for the other interconnects in the system which are not of interest for fatigue life estimation. Accordingly, the equivalent beam should be characterized such that it mimics the forces and moments of an actual interconnect for it to be used in the assembly.

To model the G-Helix with an equivalent beam approach, a simplified model is first developed that captures the general shape of the G-Helix with the solder and copper pad as depicted in Figure 7-5. The cross-section of all of the beams is rectangular in shape. One of the design constraints for the equivalent beam is that the total stand-off height has to be equivalent to the actual interconnect, solder and copper pad. The arcuate beam was divided into five beam elements while the top post was divided into two

beams, and the bottom post which would include the copper pad and solder would include two elements. Figure 7-7 displays the schematic of the equivalent beam developed.

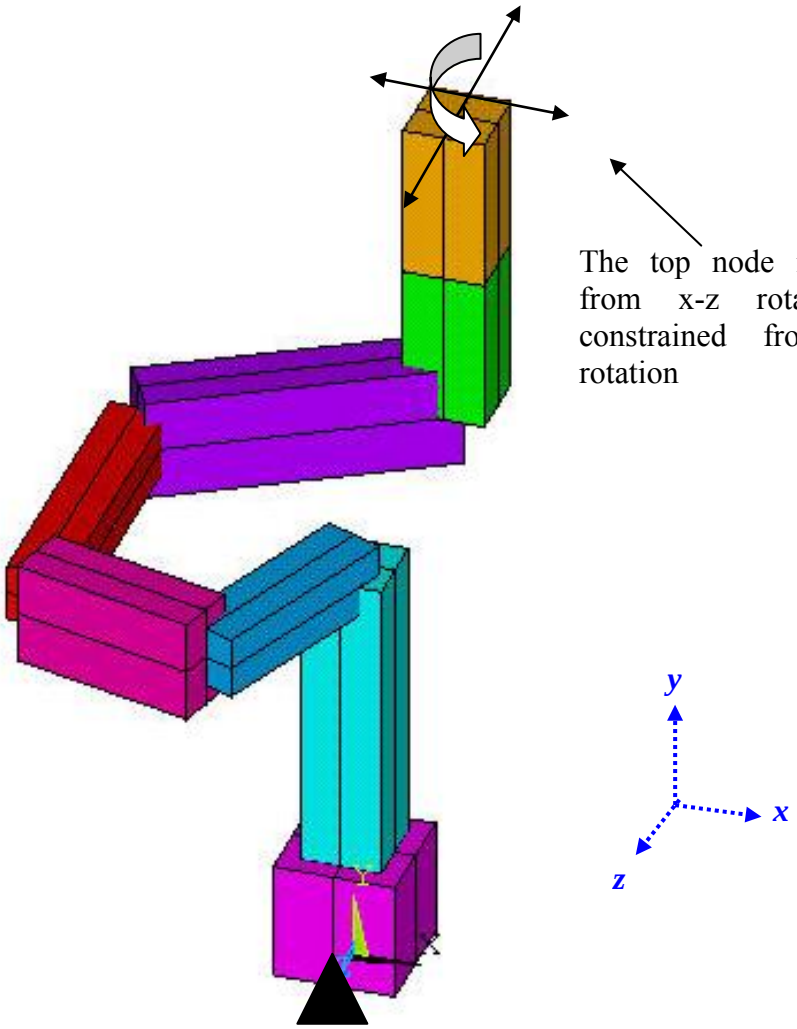
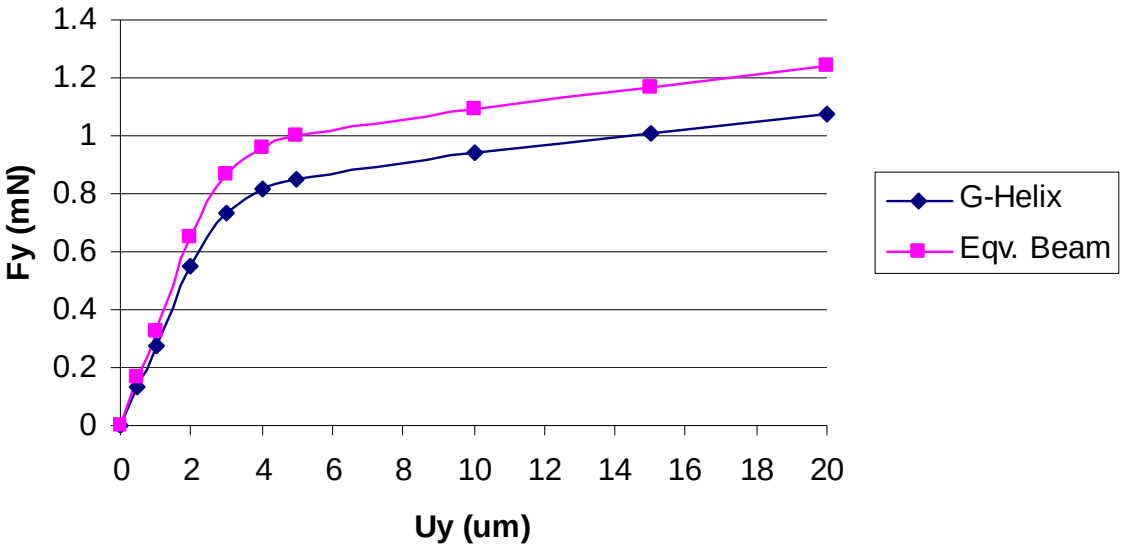


Figure 7-7: Schematic of the Equivalent Beam.

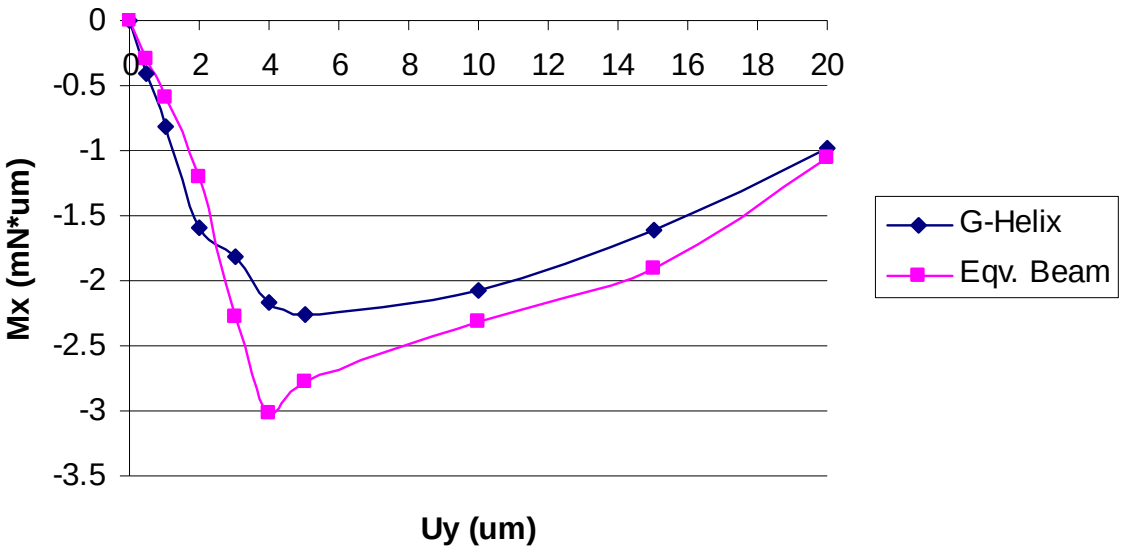
The boundary constraints on the equivalent beams shown in Figure 7-7 that the bottom beam is constrained from all degrees of freedom and the top node is coupled from in-plane (*x*-*z*) rotation and constrained from rotation in the *y*-axis. Again, the reasoning behind the coupling of the top node in the *x*-*z* plane is because to simulate the interconnect in an actual assembly. Therefore in an assembly, the surface of the top post

would be perpendicular to the surface of the silicon and PWB. The top node is also constrained from *y*-axis rotation because since the equivalent beam has a single node that interfaces with the silicon and PWB, the interconnect cannot be allowed to rotate freely about that axis which is similar to what an actual G-Helix would exhibit.

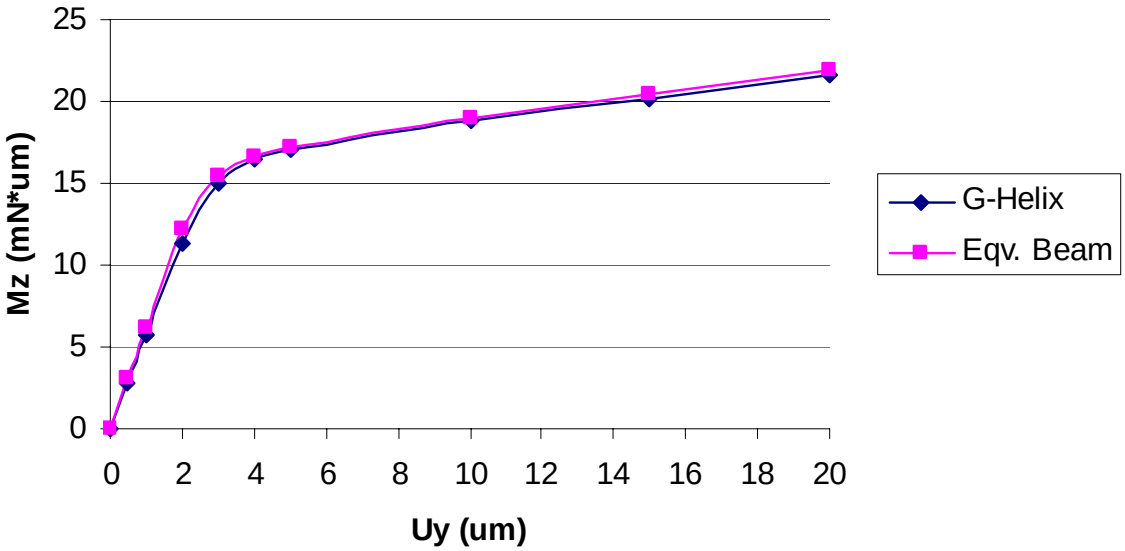
A displacement was applied in the three orthogonal directions in increments between 0.5µm - 15µm in the *x*- and *z*-direction and 0.5µm - 20µm in the *y*-direction. The values of the displacements were assumed to be within the ranges that an actual assembly would be subjected to. Other metrics that are obtained from the actual optimized G-Helix structure are the moments in the other two orthogonal directions relative to the orthogonal direction of displacement. Figure 7-6 displays and example of the plots for the force in the *y*-direction and moments in the *y*- and z-direction when a displacement was applied in the *y*-direction for the equivalent beam. The figure also display the plots of the actual G-Helix assembly to compare the difference between the two.



(a) Force in the *y*-direction vs. Displacement in the *y*-direction.



(b) Moment in the *x*-direction vs. Displacement in the *y*-direction.



(c) Moment in the *z*-direction vs. Displacement in the *y*-direction.

Figure 7-8: Numerical Simulation of the G-Helix Performance When Displaced in the y-direction.

To be able to match the equivalent beam to the actually G-Helix assembly, the material property, cross-sectional area of each individual element within the equivalent beam can be manipulated to alter the deformation characteristic of the interconnect. Also, the elements which trace the radius of the arcuate beam can be varied, but can be no greater than 100μm to prevent contact of neighboring interconnects when assembled into a package. Appendix B provides the data for each of the elements. As can be seen from Figure 7-8, the plots of the equivalent beam match well with the actual G-Helix with an average percent difference of 15 – 20%. This will subsequently be used for constructing the quarter-model assembly. With regards to the material properties and cross-sectional values used for each of the equivalent beams, they are provided in Appendix B. The responses of the deformations in the other orthogonal directions for the G-Helix and equivalent beam are also provided in Appendix B.

7.3.3. Equivalent Beam Boundary Constraints

The equivalent interconnect is comprised of beam elements with a single node that corresponds to the endpoint of the post which interfaces with solid elements for the silicon and FR-4 substrate. Therefore, to interface beam elements with solid 3D elements, relationships among different degrees of freedom need to be developed to allow the equivalent interconnect to have similar deformation characteristics as an actual G-Helix interconnect. One such association among nodal degrees of freedom between the equivalent beam and the solid elements is the application of constraint equations.

In the modeling of equivalent beams, when assembling them into a package and subjecting the assembly to thermal excursions, differential expansion and warpage will occur in the substrates. Therefore, the interconnects will deform and it should be ensured

that under deformation, the equivalent interconnects do not embed into the substrate. Constraint equations are applied at the nodes of the beams that interface with solid elements such that face of the element is perpendicular to the interconnect. Figure 7-9 visually depicts the relationship between the rotational and translational degrees of freedom.

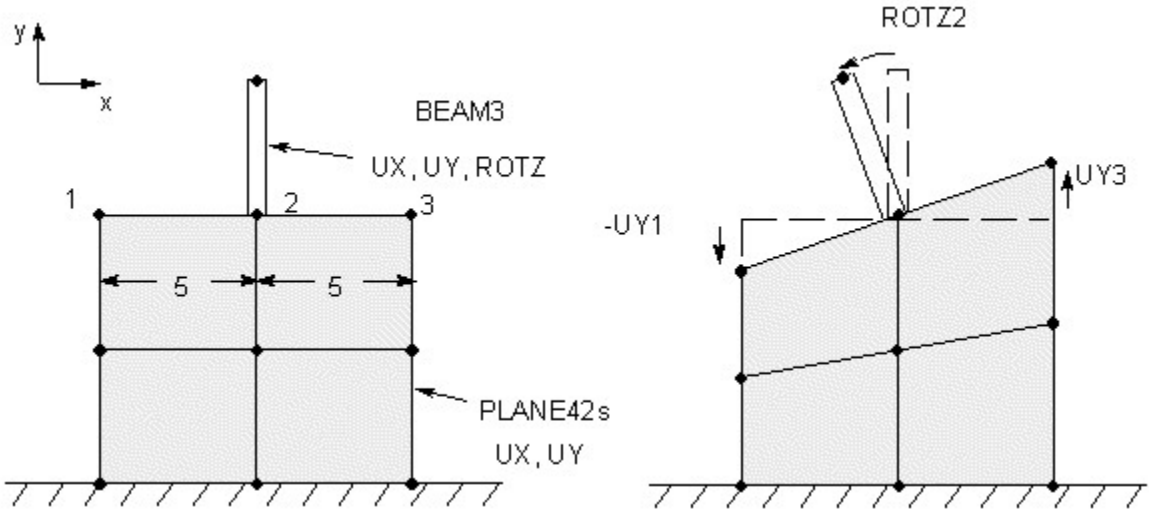
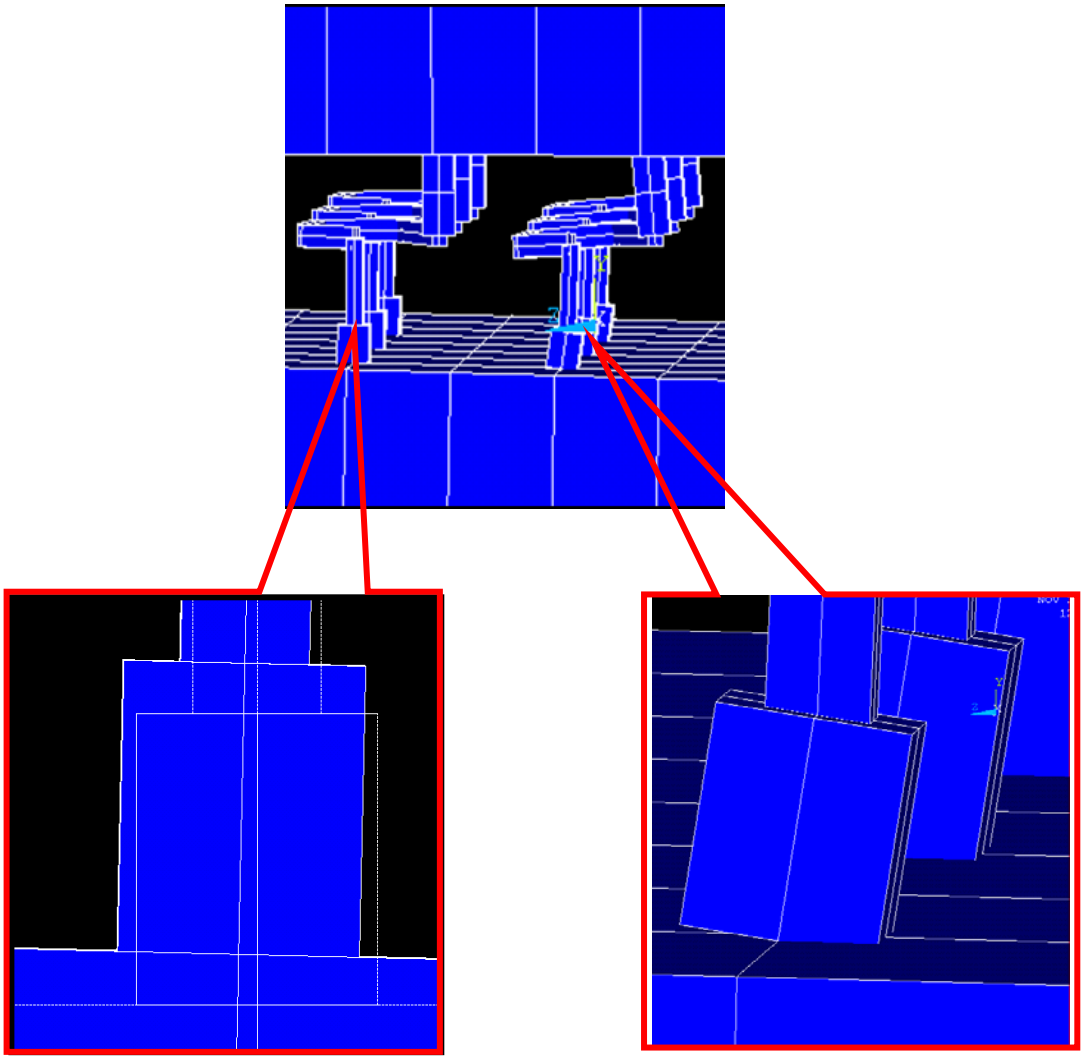


Figure 7-9: Relationship between rotational and translational degrees of freedom [ANSYS 1994].

In the figure, if no constraint equations are applied to node 2, the equivalent beam would subsequently act like a hinge which is free to rotate. Therefore, to transfer moments between the equivalent beam and the element such as an actual G-Helix interconnect would, the following constraint equation is utilized assuming that the distance between nodes 1 – 3 is 10:

$$ROT_{z,2} = \frac{(U_{y,3} - U_{y,1})}{10} \qquad 7\text{-}1$$

Another boundary constraint that was set in place for the equivalent beam is that they should not be allowed to rotate freely about the y-axis at the interface between the beam and solid element. Once the boundary constraint equations were set in place, to validate and ensure that the constraint equations perform the way that they are supposed to, a package simulation was executed where an in-plane displacement was applied. Figure 7-10 displays the effects of the constraint equations on the deformation effects of the equivalent beams.



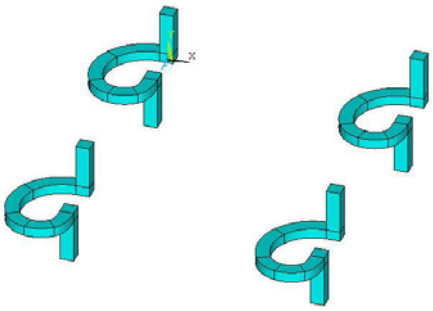
(a) Incorporate Constraint Equations (b) Without Constraint Equations

Figure 7-10: Validation of Constraint Equations.

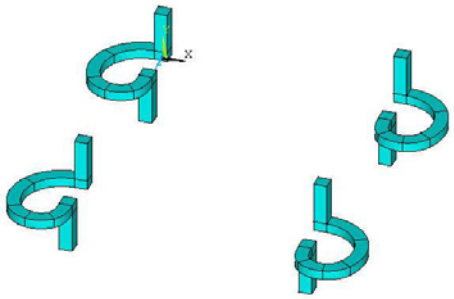
7.4. G-Helix Orientation Analysis

In a traditional flip-chip, solder bumps are rotationally symmetric. However, the G-Helix interconnects are not rotationally symmetric, and their behavior is dependent on the orientation relative to the radial axis from the neutral point of the package. As a first step, in this work, three types of orientations were investigated: uniform orientation, half-mirrored orientation, and quarter-mirrored orientation.

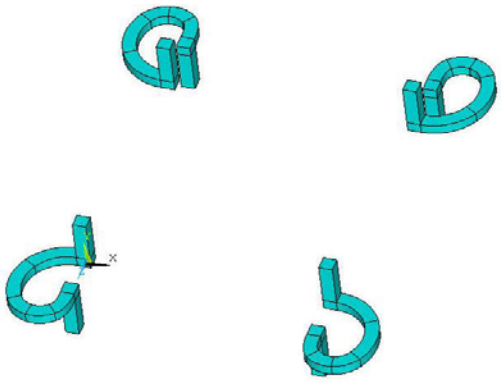
Uniform orientation is one in which all of the interconnects are oriented in the same direction across the whole die [Figure 7-11a]. Half-mirrored orientation [Figure 7-11b] is one in which the interconnects on one half of the die are the mirror image of the interconnects on the other half of the die. Quarter-mirrored orientation [Figure 7-11c] is one in which each quadrant is a mirror image of the two neighboring quadrants.



(a) Uniform orientation symmetry Model



(b) Half-mirrored orientation Model



(c) Quarter-mirrored orientation Model

Figure 7-11: Three Orientations of the G-Helix Under Analysis.

With the three different orientations, a compressive load of 1 mN is applied at the center of the package to simulate assembly of the G-Helix interconnects. It should be noted that the magnitude of stresses on the G-Helix interconnects is a relative comparison as only four interconnects were modeled. The main objective of the study is to understand the trends of how orientation effects the stress state of the G-Helix interconnects and not the actual magnitude of the stress.

7.4.1. Orientation Analysis: Compressive Load

To simulate assembly of the G-Helix interconnects a simplified model is used with four interconnects to model the three types of orientations. The boundary constraints on the four interconnects are that the base of each of the four interconnects is rigidly constrained from displacements and rotation, and a compressive load of magnitude 1 mN was applied at the center of the package. An example of the model described is shown in Figure 7-12.

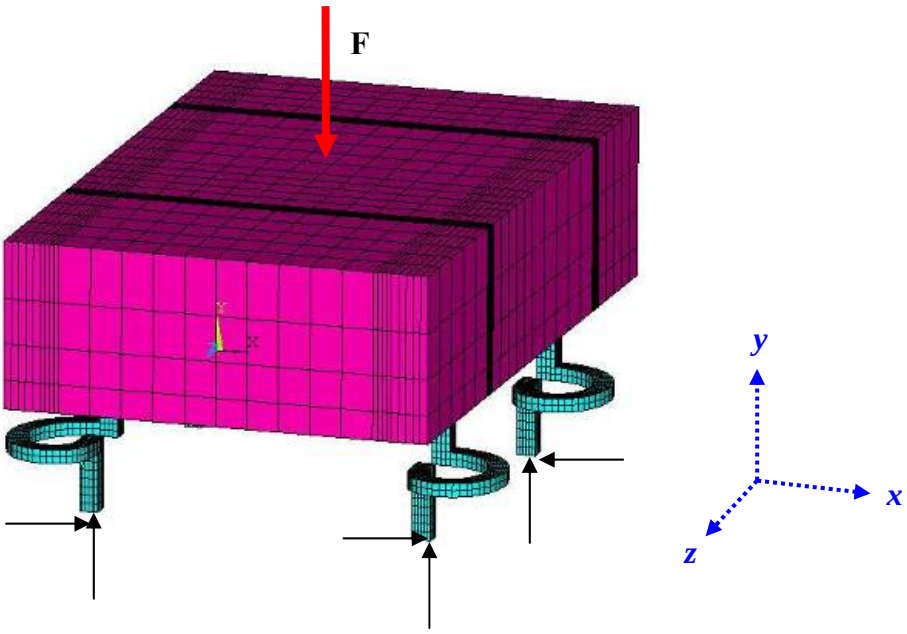
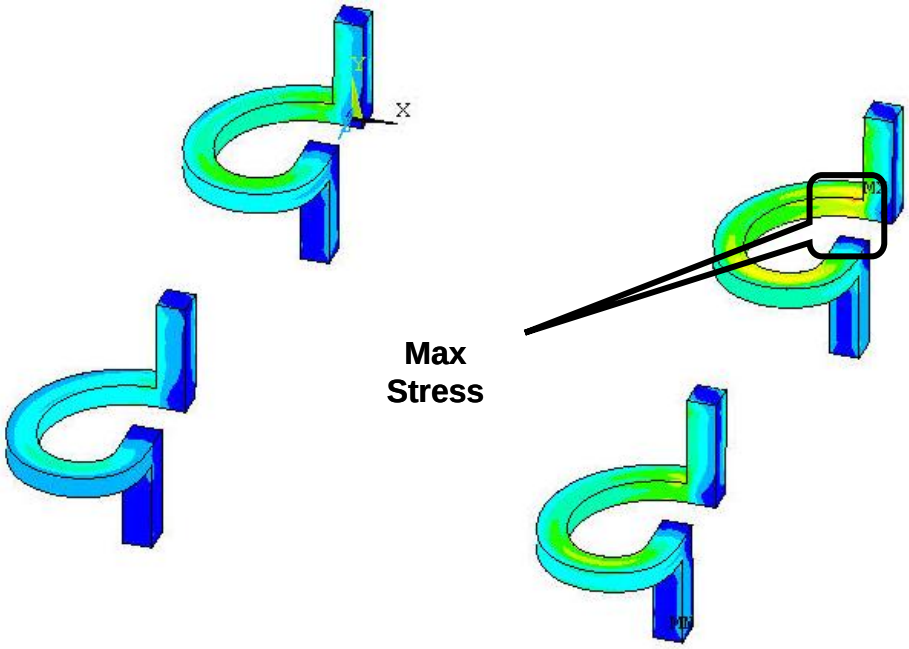


Figure 7-12: Half-mirrored Orientation Model for Compressive Load Analysis

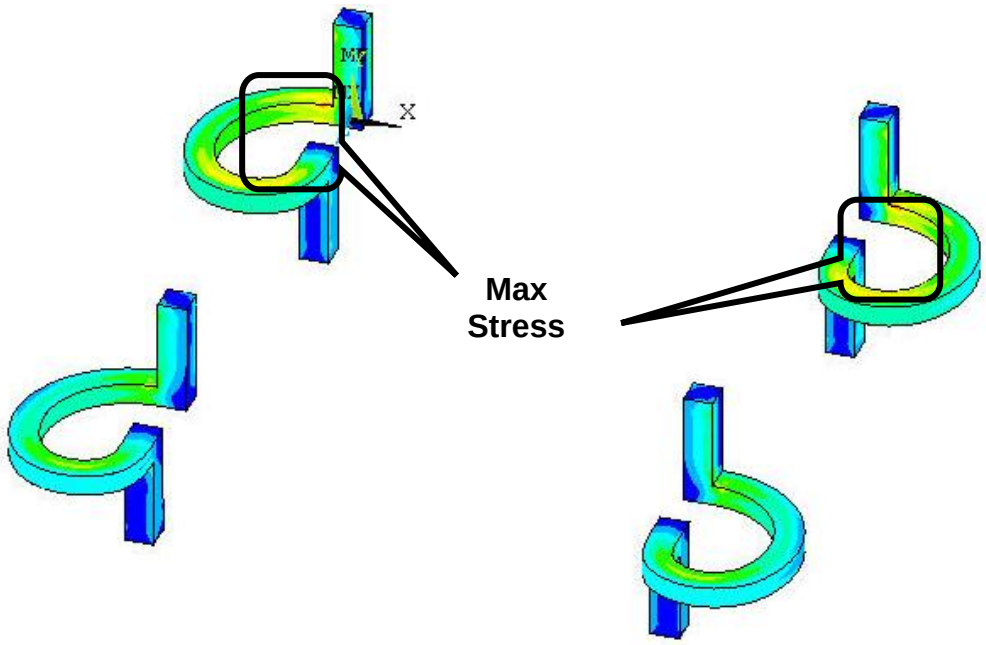
Table 7-1 displays the maximum von Mises stress in the interconnect for the various orientations and Figure 7-13 exhibits the location where the maximum von Mises stress occurs.

Table 7-1: Maximum von Mises Stress in the G-Helix Interconnects.

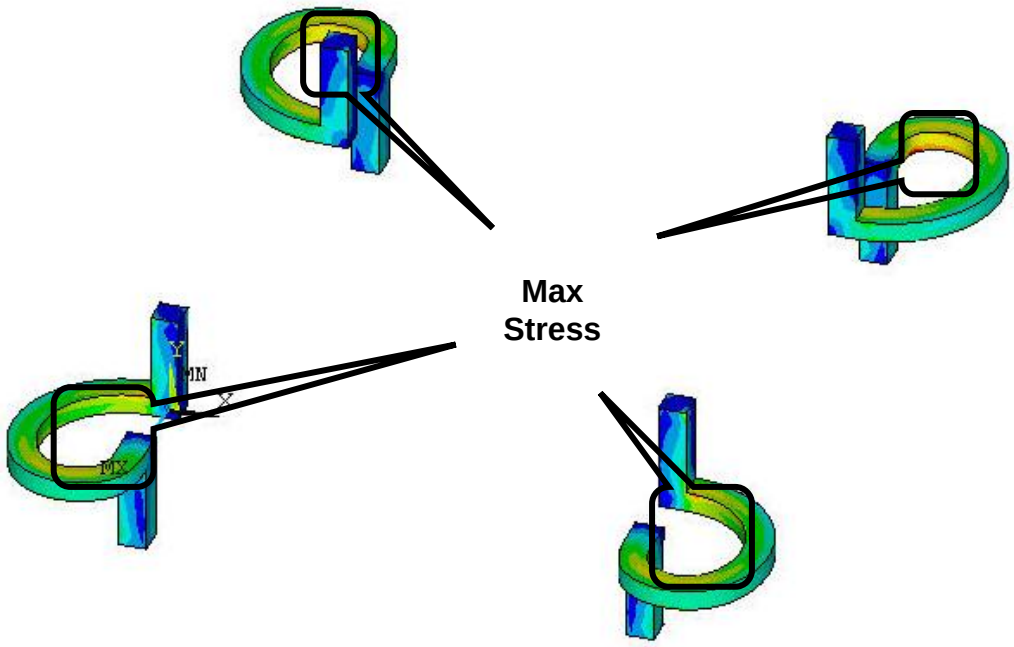
Orientation of G-Helix	**Max von Mises Stress (MPa)**
Uniform	146.6
Half-mirrored	125.5
Quarter-mirrored	112.3



(a) Uniform Orientation Symmetry Model



(b) Half-mirrored Orientation Model



(c) Quarter-mirrored Orientation Model

Figure 7-13: Location of the Maximum Stress for different orientations of G-Helix due to an Assembly Load.

The geometry of the G-Helix interconnect is such that when a vertical compressive load is applied on the vertical top post, it creates a bending moment which has M_{xx} and M_{zz} components. Of the three orientations, the quarter-symmetry orientation is such that these bending moments could be off-set by complimentary interconnects, and therefore, this orientation would produce the least amount of stress in the interconnect.

7.5. Thermo-mechanical Analysis of the G-Helix Assembly

With the numerical models developed, they are subjected to thermal cycling and in conjunction with life-prediction models the fatigue life of the G-Helix assembly can be estimated. GPD and a quarter model with equivalent beams is used to understand the thermo-mechanical reliability of the G-Helix.

To join the G-Helix interconnect to the FR-4 substrate, four different solder attach materials (63Sn/37Pb, 60Sn/40Pb, 96.5Sn/3.5Ag, and 95.5Sn/4Ag/0.5Cu) were studied through finite element modeling. Table 7-2 summarizes the melting temperature and material modeling of the four types of solders analyzed.

Table 7-2: Melting Temperature and Constitutive Behavior of Four Types of Solder.

Material	Melting Temperature (°C)	Solder Constitutive Behavior
63Sn/37Pb	183	Multilinear Kinematic Hardening with Power Law Creep
60Sn/40Pb	183	Anand's Viscoplastic Model
96.5Sn/3.5Ag	220	Anand's Viscoplastic Model
95.5Sn/4Ag/0.5Cu	220	Multilinear Kinematic Hardening with Power Law Creep

During the assembly process, the amount of solder that is attached to the G-Helix will vary. Therefore, in modeling of the attachment between the solder and bottom post of the G-Helix, the amount of the post that is embedded into the solder is studied to understand the effects of the thermo-mechanical reliability of the assembly. The amount of the copper post that is embedded into the solder is varied from 4μm - 12μm in increments of 4μm. Figure 7-14 visually depicts what was described.

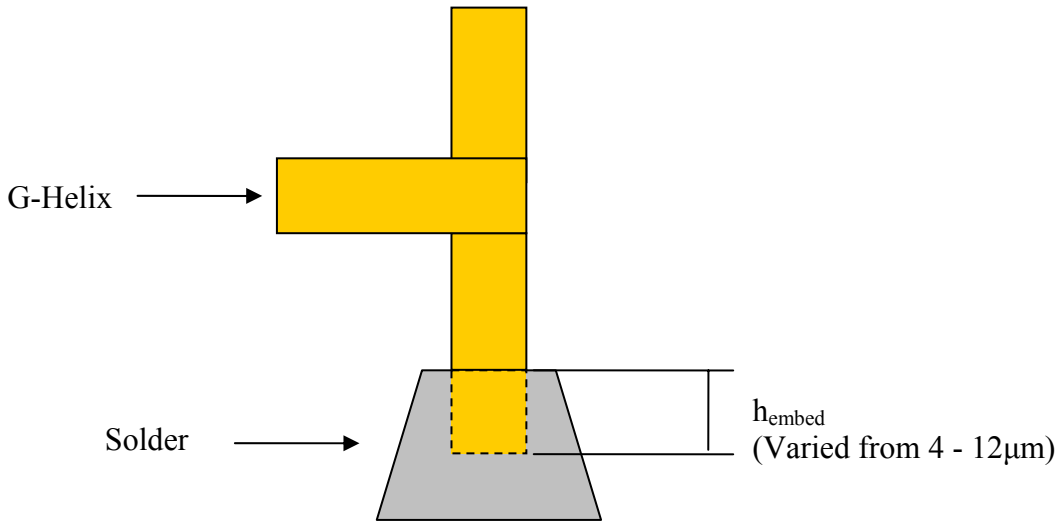


Figure 7-14: Embedding the Copper Post of the G-Helix into the Solder.

The thermal loading was simulated as follows: The package was first subjected to a load step from solder melting temperature to room temperature (20°C); it is then dwelled for about an hour at room temperature. Next, the package was subjected to accelerated thermal cycles between 0°C and 100°C with five minute dwells and a ramp rate of 10ºC/min. The stress-strain behavior stabilized after three cycles, and therefore, the results from the third cycle were used for further analysis. Figure 7-15 displays an example of the thermal loading that was simulated.

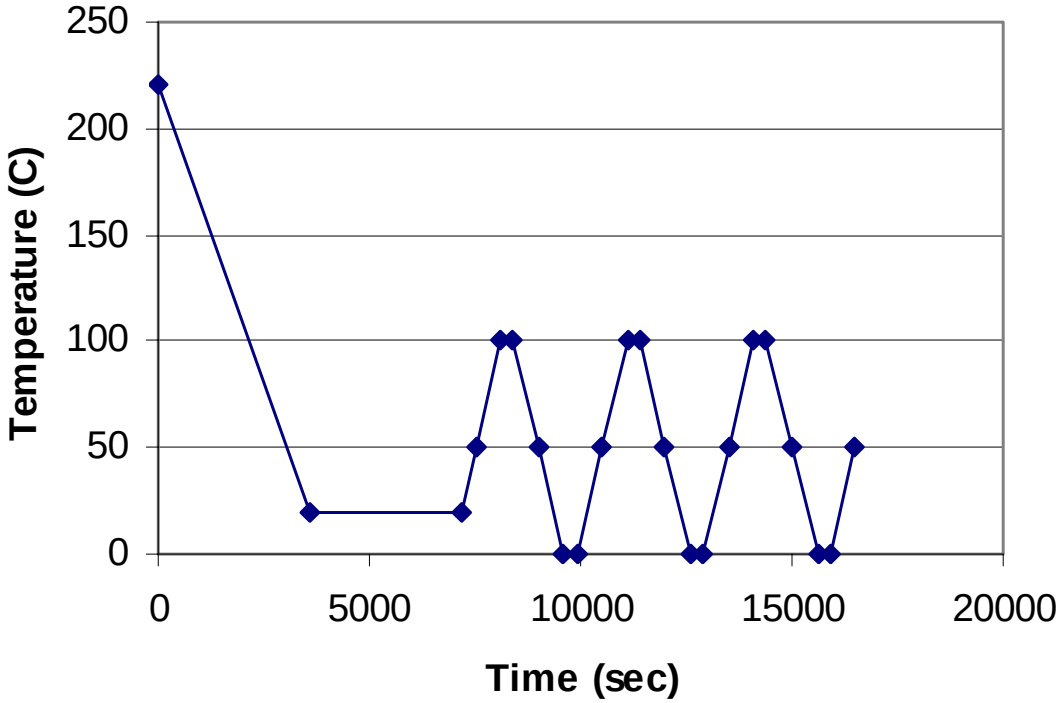


Figure 7-15: Thermal Loading Simulated.

7.5.1. GPD Results and Discussion

Once the assembly is simulated with the thermal loading, the mechanics of deformation of the compliant G-Helix interconnect is recognized and the location where maximum inelastic strain is identified. The GPD model is subjected to three thermal cycles to ensure that the stress-strain hysteresis loop stabilizes and after the third thermal cycle, the inelastic strains of the G-Helix and solder is plotted. It can be seen that the maximum plastic strain is shown to be induced in the outermost interconnect and located at the sharpest turn of the arcuate beam as shown in Figure 7-16.

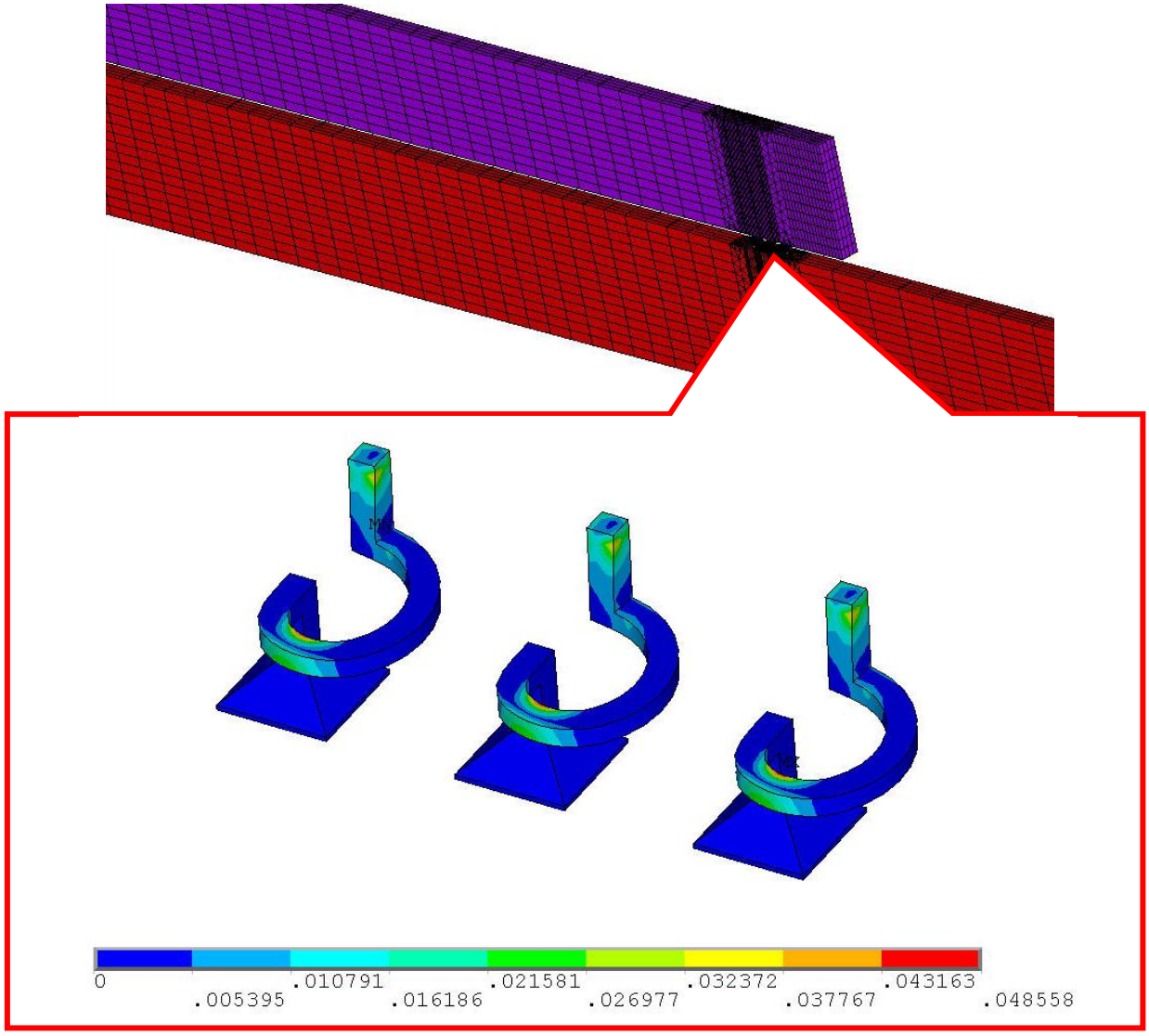
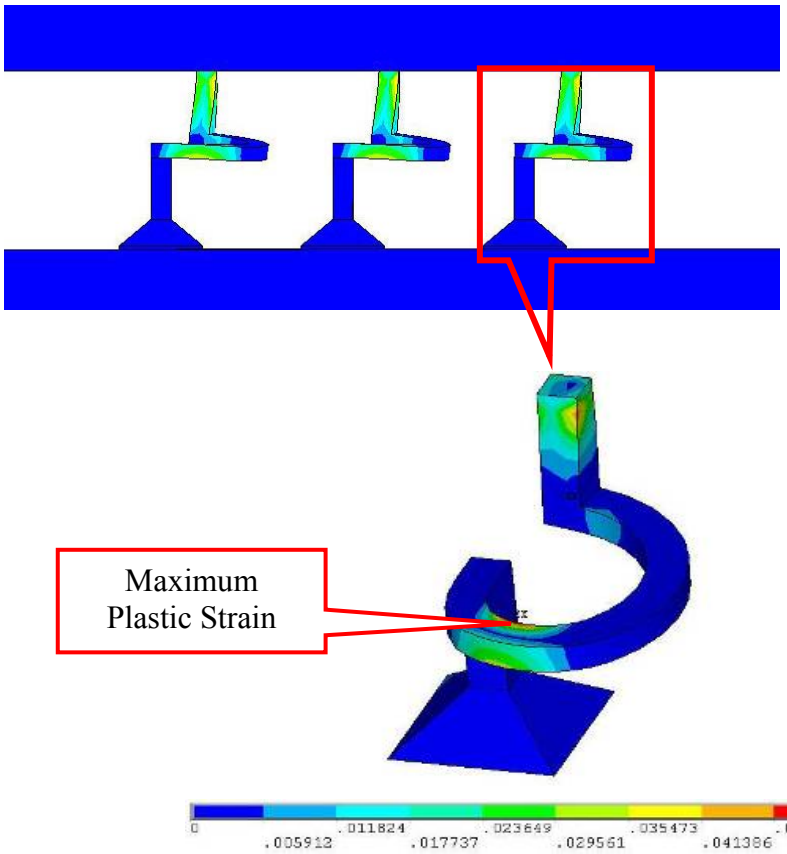
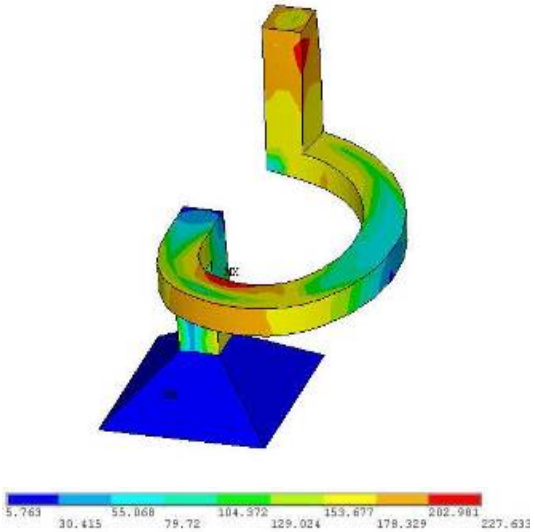


Figure 7-16: Inelastic Strain Contours After the Third Thermal Cycle For 95.5Sn/4Ag/0.5Cu.

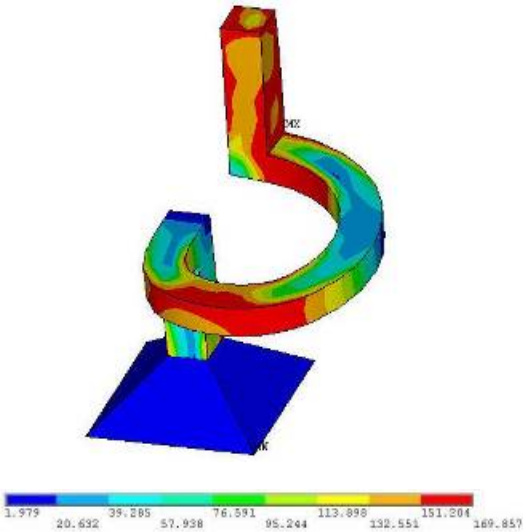
Since the outermost interconnect is where the most damage is accumulated, it is the focus for the subsequent analysis. Figure 7-17a shows equivalent plastic strain distribution at room temperature and location of the maximum plastic strain after three thermal cycles, and Figure 7-17b and Figure 7-17c shows the von Mises distribution at the end of high and low temperature dwells for 96.5Sn/3.5Ag solder with 8μm of the bottom post embedded into the solder.



(a) Equvalent plastic strain distribution after 3rd Themal Cycle



(b) T_{Low} Dwell von Mises Stress Distribution after 3rd Themal Cycle



(c) T_{Hi} Dwell von Mises Stress Distribution after 3rd Themal Cycle

Figure 7-17: Equivalent Plastic Strain and von Mises Stress Distribution for G-Helix Assembly for 96.5Sn/3.5Ag With 8µm Embedded into the Solder.

It can be seen from Figure 7-17b and Figure 7-17c that the maximum stress induced in the interconnect increase as the temperature decreases. This is because the assembly is moving away from the stress free temperature which is assumed to be at the solder melting temperature. At the end of the T_{Hi} (100°C) dwell temperature, the maximum von Mises stress is less than the yield stress of copper (σ_y = 172 MPa).

Fatigue Life of G-Helix Assembly

As can be seen in Figure 7-17a, the maximum plastic strain occurs at the outermost interconnect and located at the sharpest turn of the arcuate beam which is circled in the figure. Coffin-Manson-type equation, derived using experimental data, can be used to determine the low-cycle fatigue life of electroplated copper and the equation can be written as:

$$N_f^{-0.6} \times \varepsilon_f^{0.75} = \Delta\varepsilon_p \qquad 7\text{-}2$$

N_f: Mean cycles to failure
$\Delta\varepsilon_p$: Plastic strain range
ε_f: Fatigue ductility coefficient

Table 7-3 and Table 7-4 show the maximum plastic strain range of copper, fatigue life estimation, and failure location of G-Helix when attached with the leaded and lead-free solders. The fatigue ductility coefficient for copper was reported to vary from 0.15 to 0.3 [Prabhu 1995]. The effects of the amount of the post that was embedded into the solder is also provided in the table, and if the failure was found to be in the solder, depending on the type of solder used to attach the G-Helix to the FR-4, the corresponding fatigue model as described in Chapter 2 is used.

Table 7-3: G-Helix Packaging Fatigue Life with Leaded Solder Attach Materials and Varying the Amount of the Post Embedded into the Solder.

	63Sn/37Pb			60Sn/40Pb		
h_{embed} (µm)	**Maximum $\Delta\varepsilon_p$ (%)**	**Failure Location**	**FEM Life (N50)**	**Maximum $\Delta\varepsilon_p$ (%)**	**Failure Location**	**FEM Life (N50)**
12 µm	0.514	Copper	1040	0.506	Copper	1067
8 µm	0.493	Copper	1116	0.482	Copper	1157
4 µm	0.426	Copper	1425	0.456	Copper	1272

Table 7-4: G-Helix Packaging Fatigue Life with Lead-Free Solder Attach Materials and Varying the Amount of the Post Embedded into the Solder.

	96.5Sn/3.5Ag			95.5Sn/4Ag/0.5Cu		
h_{embed} (µm)	**Maximum $\Delta\varepsilon_p$ (%)**	**Failure Location**	**FEM Life (N50)**	**Maximum $\Delta\varepsilon_p$ (%)**	**Failure Location**	**FEM Life (N50)**
12 µm	0.473	Copper	1195	0.474	Copper	1191
8 µm	0.453	Copper	1285	0.468	Copper	1218
4 µm	0.429	Copper	1406	0.426	Copper	1420

Using Engelmaier's model, equation 2-1, and with 4 - 12µm embedded into the solder, the G-Helix has the potential to withstand over 1000 thermal cycles. It can be seen from the above table that embedding the post into the solder does have an effect on the fatigue life of the assembly. When the amount of the G-Helix post that is embedded into the solder decreases, it subsequently increases the fatigue life of the assembly. This is because the total stand-off height of the assembly increases. However, as the plastic strain range decreases in the copper interconnect because the stand-off height increases, the inelastic strain in the solder increases.

7.5.2. Quarter Model Results and Discussion

Building on top of what is understood from a GPD model, a quarter model package is constructed to understand be able to run a numerical model for the G-Helix assembly, it includes equivalent beams for all the interconnects except the one of interest for fatigue life estimation. In a flip chip/WLP assembly, the interconnect of interest is the one that is the furthest from the DNP as it will experience the most displacement and subsequently the most damage. This corresponds to the interconnect at the corner of the package as shown in Figure 7-18.

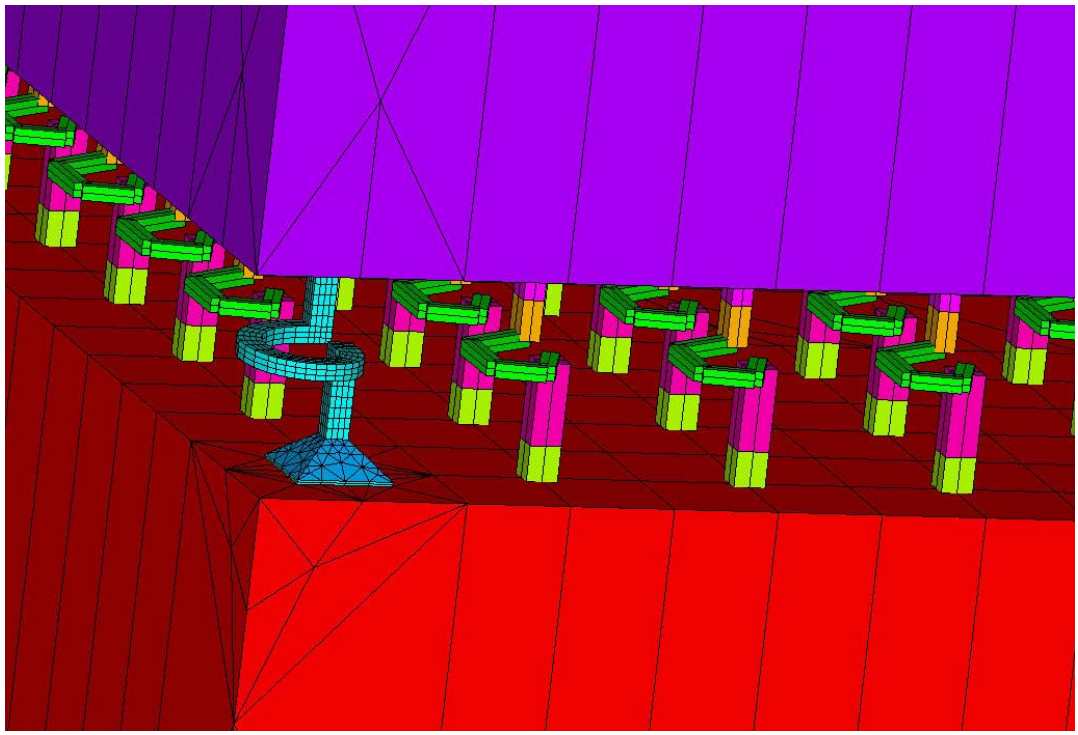


Figure 7-18: Quarter model incorporating Equivalent Beams.

After the third thermal cycle, the inelastic strain is plotted, and as it can be seen, the maximum strains are induced in the copper arcuate beam structure. The location of the maximum plastic strain induced in the G-Helix is circled in Figure 7-19.

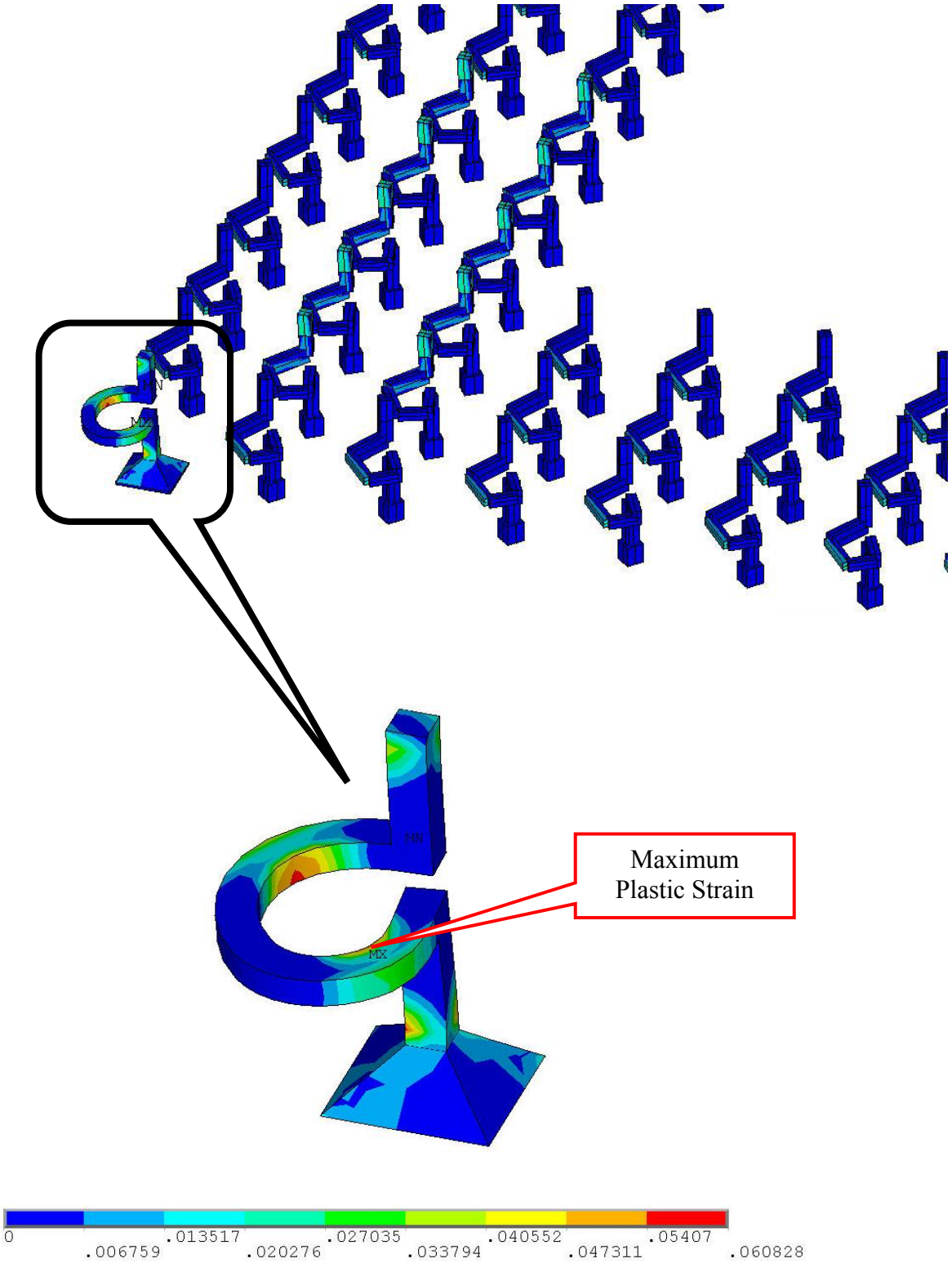


Figure 7-19: Inelastic Strain Distribution After 3rd Thermal Cycle.

Comparing the location of the plastic strains for the quarter model versus the GPD model, they are relatively in the same location. Using Engelmaier's equation, Equation 2-1, the fatigue life of the G-Helix at the critical region can be estimated. The value is compared with the same scenario for the GPD model. Table 7-5 displays the comparison between the two.

Table 7-5: Comparison of Fatigue Life for 96.5Sn/3.5Ag Solder with 8μm of the Bottom Post Embedded into the Solder.

	GPD Model			**Quarter Model**		
h_{embed} (μm)	**Maximum $\Delta\varepsilon_p$ (%)**	**Failure Location**	**FEM Life (N50)**	**Maximum $\Delta\varepsilon_p$ (%)**	**Failure Location**	**FEM Life (N50)**
8 μm	0.453	Copper	1285	0.584	Copper	845

As can be seen from the two numerical simulations, the quarter model predicts a lower fatigue life compared to the GPD model. The reasoning behind this could be due to the fact that when the G-Helix is modeled in a GPD, the nodes on both sides of the slice is coupled so that they have uniform expansion. Therefore, it assumes an array of three interconnects in the two faces of the slice so the package would appear to have interconnects only on two sides of the package. The array of interconnects in the other two sides are not captured in the model which would provide warpage in the other direction. Therefore, the model would have warpage that is shaped like a bowl in the quarter model instead of a parabola in the GPD model. Due to this effect, the estimated fatigue life of the quarter model produces a lower number of cycles to failure.

CHAPTER 8

SUMMARY AND FUTURE WORK

8.1. Summary and Contributions

The following is a summary of the contributions achieved through this research:

- A scalable technology has been developed and demonstrated
- The developed technology is wafer-level
- Appropriate for low-K dielectric/copper dies due to high compliance
- Reworkable; without the use of underfill
- The interconnects are environmentally friendly when lead-free solders are used for solder attachment
- 100 micron has been successfully fabricated as part of this work
- 20 mm dies which the interconnects are fabricated on is in-line with ITRS 2003 projections
- The fabricated interconnects have been subjected to excessive deformation, and they appear reliable.
- Assembly process/methodology has been developed
- The assembled test vehicles are being reliability assessed, and preliminary results are positive.

- In parallel to the experiments, physic-based models have been developed; both quarter symmetry with equivalent beam elements as well as GPD models developed; predicted reliability is good

8.2. Future Work

Some other gaps are identified that require investigation or further improvement. Some recommendations for future work are outlined here:

- Investigate into alternative photoresist to SU-8. Removal of this material requires a long dry etch process. An ideal alternative material that can be used for the first layer would be one that can withstand temperatures ~200°C and be easily etched away with a dry or wet etch process.
- Cost Analysis to quantitatively measure the competitiveness of the G-Helix to conventional solder bump technology with underfill.
- Investigate into alternative geometries to improve the mechanical compliance.
- Reduce the number of processing steps to fabricate a compliant interconnect structure.
- Understand the capability to propagate a high frequency signal through the G-Helix assembly.
- Empirically characterize the electrical parasitics of the interconnect.
- Scale the interconnects down to pitch scales of sub-100μm pitch and assembling them onto organic substrates.

- Understand the capability of stencil printing solder on the board and assembling the interconnects.
- Investigate assembling lead-free solders with either electroplating solder onto the end of the post, or applying the solder onto the board side by stencil printing.
- Material characterization of thin-film materials.
- Assemble the compliant interconnects utilizing lead-free solders.
- Assemble more dies to obtain a larger sample size to extrapolate the mean fatigue life of the interconnects.
- Perform failure analysis on the interconnects after thermal cycling.
- Understand the effects on grain growth of the copper material that is used to electroplate the G-Helix when it is subjected to multiple reflows.
- Investigate chemical mechanical planarization of the arcuate beam so as to decrease the surface roughness and improve electrical characteristics of the G-Helix especially at high frequencies where skin effect takes into effect.

APPENDIX A

COPPER PLATING RECIPE

Copper Plating Recipe

The following recipe is a high throughput, large grain copper bath. Below is the recipe for 9L of the bath:

- $CuCl_2$ = 0.6g
- $CuSO_4$ = 1100g
- H_2SO_4 = 25.6ml
- H_2O = 9L

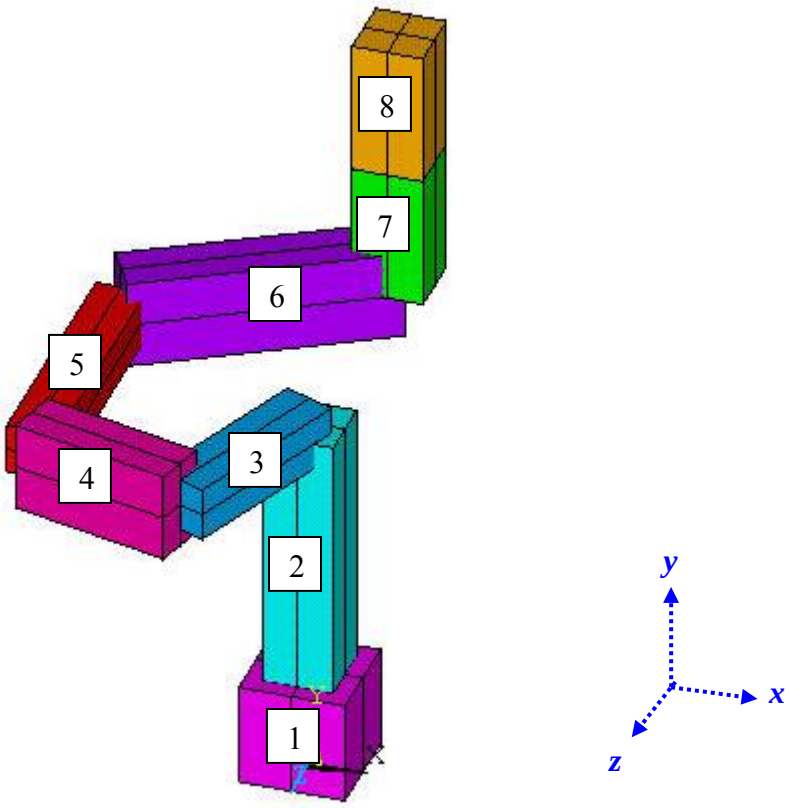
To produce smaller grained copper with roughness of ±2–3μm, a high acidic bath can be used, and the recipe for the bath is as follows:

- $CuSO_4$ - 73 g/l
- H_2SO_4 - 210 g/l (note: 1 cc of 98% H_2SO_4 is not equal to 1g!)
- Cl 67mg/l (This can be $CuCl_2$ or HCl)
- H_2O – Fill up to the 1L mark

APPENDIX B

EQUIVALENT BEAM CHARACTERIZATION

Dimensions and Material Properties of Equivalent Beam



Section	E (GPa)	σ_y (MPa)	Tangent Modulus (MPa)	ν	B (μm)	H (μm)
1	121	172	1750	0.3	15	15
2	121	172	1750	0.3	10	10
3	70	190	1750	0.3	7.8	7.8
4	90	240	1750	0.3	13	8
5	100	200	1750	0.3	7.2	7.2
6	70	190	1750	0.3	13	8
7	110	160	1750	0.3	10	10
8	110	160	1750	0.3	10	10

Displacement in the *x*-Direction G-Helix Results

U_x (μm)	F_x (mN)	M_y (mN-μm)	M_z (mN-μm)
0	0	0	0
0.5	0.24335	1.66	13.07
1	0.48431	3.32	26
2	0.92562	6.12	49.73
3	1.12573	7.61	61.08
4	1.188	7.88	65.2
5	1.23457	7.96	68.4
7.5	1.32646	8.1	74.3
10	1.40061	8.35	78.7
12.5	1.46684	8.74	82.47
15	1.52997	9.12	86.12

Displacement in the *x*-Direction Equivalent Beam Results

U_x (μm)	F_x (mN)	M_y (mN-μm)	M_z (mN-μm)
0	0	0	0
0.5	0.19364	0.91	10.44
1	0.3879	1.85	20.93
2	0.76848	4.03	41.74
3	0.89875	6.57	49.47
4	0.95199	7.04	53.09
5	0.99827	7.69	56.73
7.5	1.10254	9.09	64.44
10	1.1491	8.82	67.28
12.5	1.21901	9.21	71.8
15	1.27221	9.28	74.64

Displacement in the *y*-Direction G-Helix Results

U_y (μm)	F_y (mN)	M_x (mN-μm)	M_z (mN-μm)
0	0	0	0
0.5	0.1374	-0.4	2.86
1	0.27488	-0.81	5.71
2	0.54862	-1.6	11.35
3	0.72954	-1.82	14.97
4	0.81366	-2.16	16.51
5	0.85063	-2.25	17.12
10	0.94194	-2.07	18.77
15	1.01039	-1.61	20.18
20	1.07845	-0.99	21.57

Displacement in the *y*-Direction Equivalent Beam Results

U_y (μm)	F_y (mN)	M_x (mN-μm)	M_z (mN-μm)
0	0	0	0
0.5	0.16307	-0.3	3.08
1	0.32603	-0.59	6.16
2	0.64689	-1.21	12.15
3	0.86882	-2.27	15.51
4	0.96088	-3.01	16.65
5	0.99941	-2.77	17.18
10	1.08985	-2.32	18.99
15	1.16569	-1.9	20.44
20	1.24361	-1.06	21.85

Displacement in the *z*-Direction G-Helix Results

U_z (μm)	F_z (mN)	M_x (mN-μm)	M_y (mN-μm)
0	0	0	0
0.5	0.40243	-21.57	-6.12
1	0.78785	-42.13	-11.87
2	1.36161	-72.81	-21.22
3	1.50898	-81.45	-23.72
4	1.56628	-84.93	-24.69
5	1.60871	-87.63	-25.33
7.5	1.68727	-92.64	-26.31
10	1.74763	-96.54	-26.84
12.5	1.79768	-99.92	-27.08
15	1.84083	-102.96	-27.07

Displacement in the *z*-Direction Equivalent Beam Results

U_z (μm)	F_z (mN)	M_x (mN-μm)	M_y (mN-μm)
0	0	0	0
0.5	0.33688	-18.18	-5.22
1	0.6733	-36.31	-10.38
2	1.06545	-57.74	-18.47
3	1.14485	-63.02	-20.67
4	1.17635	-65.91	-21.27
5	1.21403	-69.32	-21.85
7.5	1.25951	-73.2	-22.51
10	1.29395	-75.7	-22.62
12.5	1.32913	-78.24	-22.74
15	1.35187	-79.8	-22.52

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